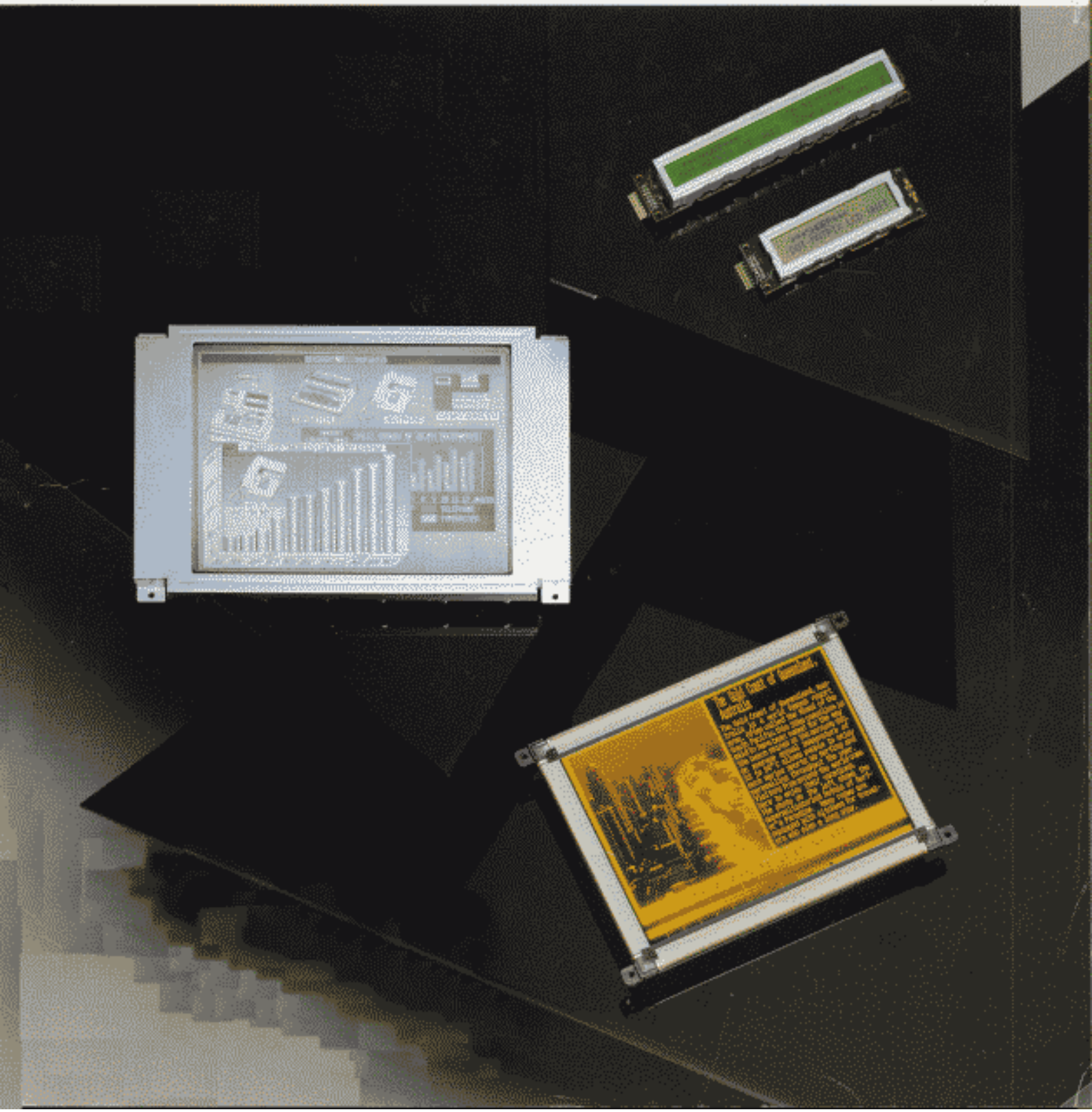
SHARP

Flat Panel Displays

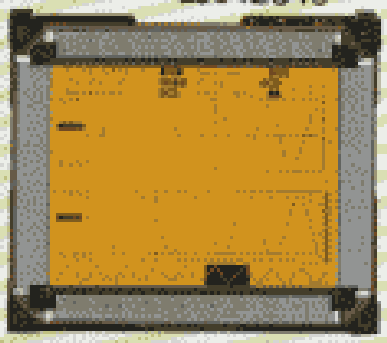
LCD Units/EL Display Units



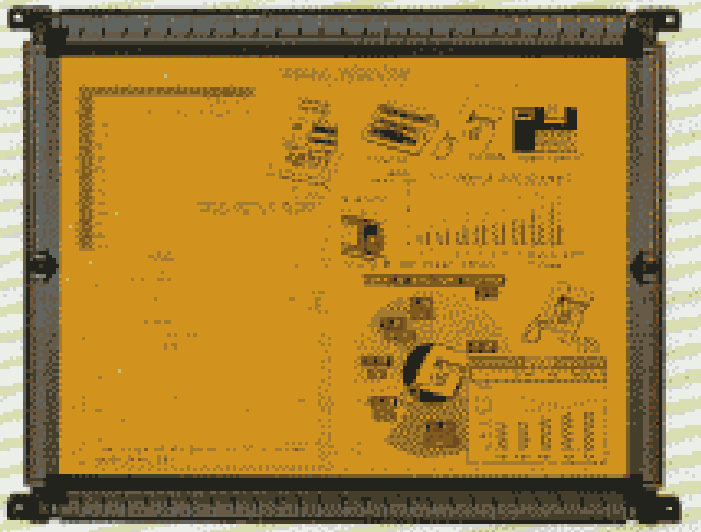
EL
Display Units

SHARP's EL display units feature clear, flicker free images with a 160° wide viewing angle. Now you can take advantage of SHARP's advanced EL technology in both high resolution (1024 × 768) and 16 gray scale displays. SHARP's EL display units are the first choice for ruggedized workstation, factory automation and transportable computer type applications.

LJ64ZU49



LJ320U27



LJ024U33

Grid compass computer

Programmable controller

Table of EL Display Units

Display format W × H(Dot)	Dot pitch W × H (mm)	Model No.	Gray scale (16 levels)	Detachable DC/DC converter	Unit outline dimensions W × H × D (mm)	Weight (g)
320 × 240	0.375 × 0.375	LJ320U21			178.5 × 148.5 × 34	600
320 × 256	0.3 × 0.3	LJ320U27			130 × 110 × 33	400
512 × 128	0.35 × 0.35	LJ512U21			228.5 × 108.5 × 34	600
512 × 256	0.375 × 0.375	LJ512U32		●	246 × 148 × 16.9/32.5*	480/540*
640 × 200	0.3 × 0.3	LJ640U25			238 × 108 × 36.6	600
	0.3 × 0.42	LJ640U23			228.5 × 148.5 × 35	650
	0.3 × 0.42	LJ640U30			228.5 × 148.5 × 35	650
	0.3 × 0.6	LJ640U24			228.5 × 158.5 × 35	750
640 × 400	0.3 × 0.3	LJ640U32		●	246 × 158 × 15.5/31.5*	480/540*
		LJ64ZU31	●	●	246 × 158 × 20.0/34.0*	535/600*
640 × 480	0.3 × 0.3	LJ640U48			246 × 180 × 25	700
		LJ64ZU49	●	●	246 × 180 × 20.0/34.0*	620/700*
720 × 400	0.3 × 0.3	LJ720U22			270 × 168 × 25.5	850
1,024 × 768	0.25 × 0.25	LJ024U33		●	310 × 238 × 15/31*	1,050/1,200*

*Including DC/DC converter

Table of Active Matrix Color TFT-LCD Modules

Application	Screen size (Inch)	Model No.	Number of pixel W × H(Pixels)	Dot pitch W × H (mm)	System	Pixel configuration	Color	Backlight	Video input signal*
AV	3	LQ323Y11	382 × 234	0.161 × 0.190	NTSC	Delta	Full color	—	Alternated analog RGB
		LQ323P07			PAL			—	Alternated analog RGB
	4	LQ4RB11	383 × 234	0.214 × 0.264	NTSC/PAL			—	Alternated analog RGB
		LQ4RE01	479 × 234	0.171 × 0.264	NTSC/PAL			—	Alternated analog RGB
		LQ4RA01			NTSC/PAL			Built-in	Analog RGB
		LQ4NC01			NTSC			Built-in	Composite
	5.7	LQ6RA01	720 × 240	0.158 × 0.365	NTSC/PAL			Built-in	Analog RGB
		LQ6NC01			NTSC			Built-in	Composite
	8.6	LQ9NE01	960 × 456	0.181 × 0.286	NTSC			—	Alternated digital RGB
OA	10.4	LQ10D01	640 × (RGB) × 480	0.33 × 0.33	—	Stripe	512	Built-in	Alternated digital RGB
		LQ10D02			—		8	Built-in	Alternated digital RGB

*Video input signal

- Alternated analog RGB: Alternated separate analog RGB video signals.
- Alternated digital RGB: Alternated separate digital RGB video signals.
- Analog RGB: Separate analog RGB signals.
- Composite: Standard composite video signals.

Detailed specifications for color TFT-LCD modules are not included in this catalog.
For more information, please contact our sales department.

(Ta=25°C)

Luminance (fL)	Supply voltage (V)	Power consumption (W)	Remark	Model No.	Page
30	+5, +15	8		LJ320U21	96
30	+5, +12	5	+5V, +15V type is also available. (LJ320U26)	LJ320U27	98
33	+5, +15	6		LJ512U21	100
34	+5, +12	7	+5V, +15V type is also available. (LJ51AU27)	LJ512U32	102
34	+5, +12	10	Extended temp. range type is also available. (LJ640U80) +5V, +15V type is also available. (LJ640U21)	LJ640U25	
30	+5, +15	10		LJ640U23	104
30	+5, +15	10		LJ640U30	
30	+5, +15	10		LJ640U24	
34	+5, +12	11	+5V, +24V type is also available. (LJ640U31)	LJ640U32	108
30	+5, +24	18		LJ64ZU31	110
30	+5, +24	17		LJ640U48	112
30	+5, +24	22		LJ64ZU49	114
30	+5, +15, +25	13		LJ720U22	116
32	+5, +24	31		LJ024U33	118

Note 1) Display color: Orange-yellow (Peak wavelength 585 nm)
Viewing angle: 160°

Note 2) Unless otherwise specified, typical values are shown.

EL Display Units

■ Numbering System

1. Basic Type

LJ○○○ U ○○

Serial number

Number of horizontal dots
(In case of large size unit,
lower three fitures)

Exception: LJ51AU27 (LJ512U27 series model)

1. Gray Scale Type

LJ○○ ZU ○○

Serial number

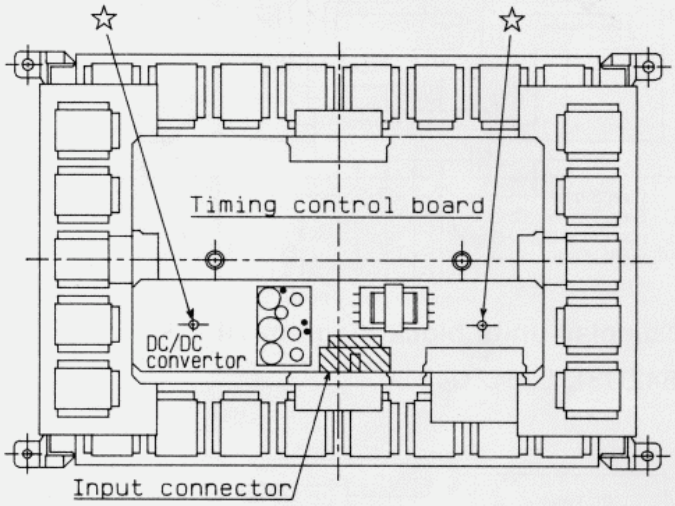
Number of horizontal dots
(Upper two figures)

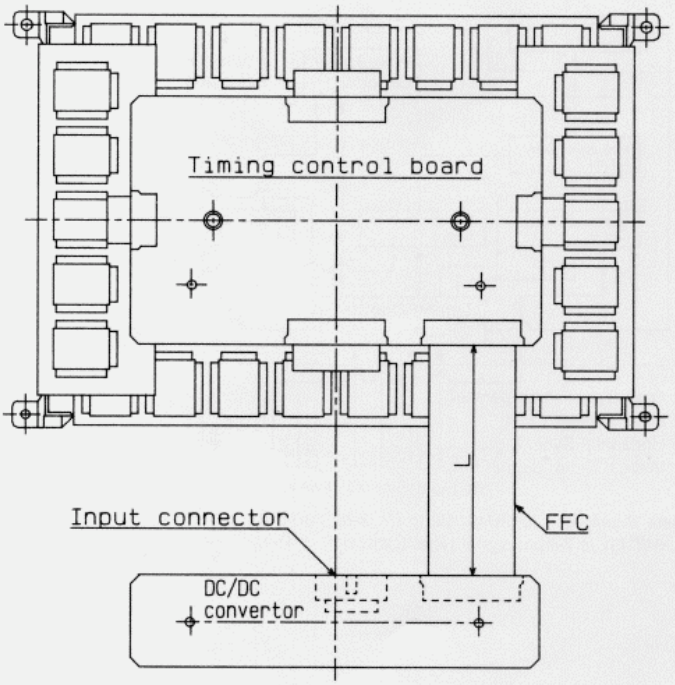
■ Detachable DC/DC Converter

The cable and converter can either be mounted on the rear of the unit or trail outside. This structure makes the unit thinner and allows greater flexibility in assembly.

Detachable DC/DC Converter

Outline dimensions (Example: LJ64ZU31)



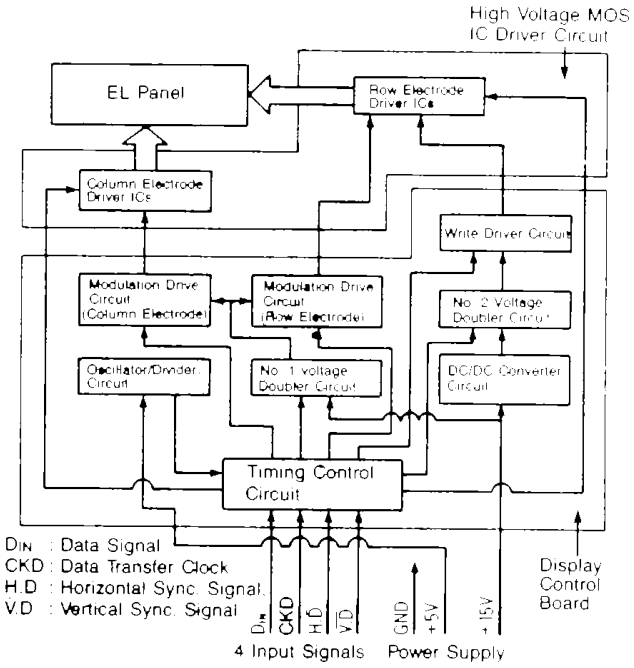


(unit: mm)

■ Block Diagram

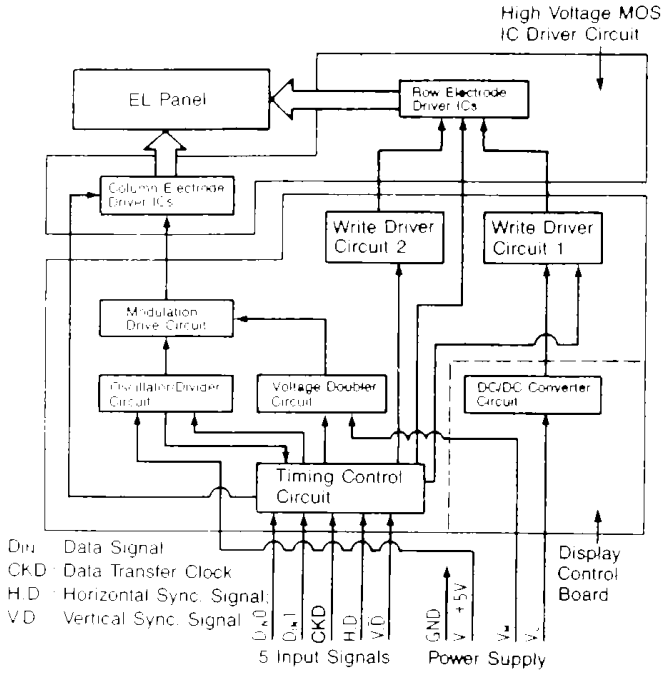
EL display units block diagram I

LJ320U21, LJ320U26, LJ512U21, LJ640U23, LJ640U24, LJ640U30



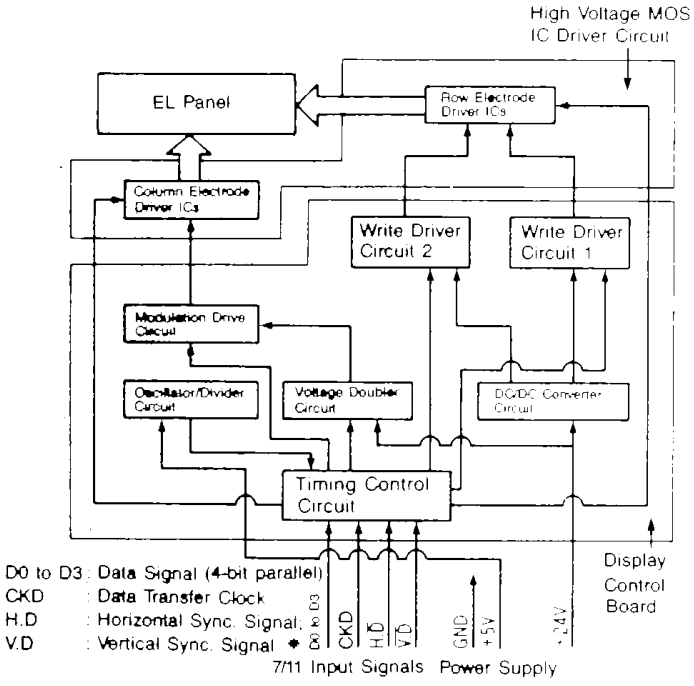
EL display units block diagram II

LJ640U48, LJ512U32*, LJ640U32, LJ640U25*, LJ024U33*



EL display units block diagram III

LJ64ZU31, LJ64ZU49



*Data Signal for LJ64ZU49: D0 to D7 (8-bit parallel)
*LJ64ZU31 is 7-input signal type; LJ64ZU49 is 11-input signal type.

1 *Models with a detachable DC/DC converter (marked with broken lines).
The maximum length of the flexible cable between the unit and the converter is 5 to 6 cm. (Refer to the specifications for details.)

2 *Model with a separated DC/DC converter (marked with broken lines).
V_M: Two types of EL display units are available, of which one type requires V_M while the other uses V_D in place of V_M (not requiring V_M).
Depending on the type of EL display unit, the values of V_D and V_M are +12V or +24V.
(Refer to the specifications for details.)

Since data signal input differs by each model, please refer to each specifications.

- Power supplies --- V_L : For logic circuit
  V_D : For panel drive
  V_M : For modulation drive circuit

■ Explanation of the Interface Signal

Signal Name	Input/Output	External Connection	Function
CKD or XSCL*1	Input	Controller	Data transfer clock This signal controls sampling and transfer of data signal.
D_{IN}*2	Input	Controller	Data signal This signal is sampled at the rising edge of each data transfer clock pulse. Data is shifted in from right to left.
UD0 to 7*1 LD0 to 7	Input	Controller	Data signal 8 bits from UD0 to UD7 are data for the upper part of the display panel and 8 bits from LD0 to LD7 are data for the lower part of the display panel. Sampled at the falling edge of the data transfer clock, this data is transferred in sequence row from right to left as 8-bit data. The data is displayed when the logic is "H" and is blanked when the logic is "L".
LP*1	Input	Controller	Latch pulse This signal controls the timing of line-at-a-time scanning and the latch timing of the data side shift register. When the logic is "H", the output of the latch circuit is directly sent to the output buffer. When the logic is "L", the preceding data is latched.
H.D	Input	Controller	Horizontal sync. signal This signal controls the timing of line-at-a-time scanning. The display data remain in effect while the logic is "H" and blanked when the logic is "L".
V.D or D_{IN}*1	Input	Controller	Vertical sync. signal This signal controls frame frequency. Frame starts when the logic rises to "H" from "L".
V_D V_L	Input	Power Supply	Power supply

*1 LJ024U33

*2 In case of 5-input type: $D_{IN}0$, $D_{IN}1$
7-input type: D0 to D3
11-input type: D00 to D03, D10 to D13

■ Options

EL display unit and interface circuit boards

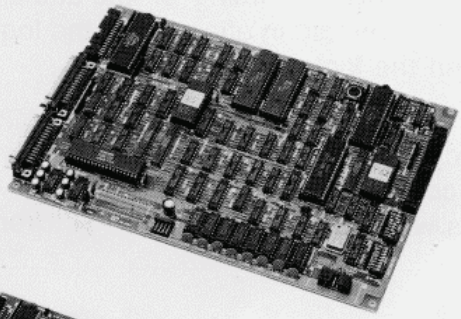
Designed as an interface circuit board between the host computer and EL display unit, the LJ232F01/02 are feature functions that generate display signals for EL displays. The boards are commonly used for interfacing both coded (characters) and full graphic signals. They are intelligent high-performance interface circuit boards provided with Z80 CPU, KANJI ROM, RS-232C i/o port and 8-bit parallel i/o port.

Interface circuit board / EL display unit	LJ232F01	LJ232F02
LJ320U21	•	
LJ320U27	•	
LJ512U21	•	
LJ512U32		•
LJ640U23	•	
LJ640U24	•	
LJ640U25	•	
LJ640U30	•	
LJ64ZU31	—	
LJ640U32		•
LJ64ZU49	—	
LJ640U48	—	
LJ024U33*	—	
Remarks	For coded/full graphic signals.	

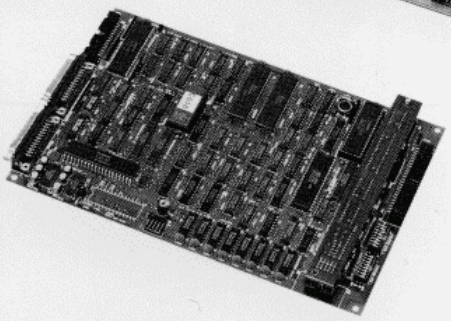
Note: Dedicated CRTC and flat panel display controller V6388 (mfd. by Yamaha Co., Ltd.) can be connected to the EL display unit. (** excl. LJ024U33).

Interface circuit board

LJ232F01

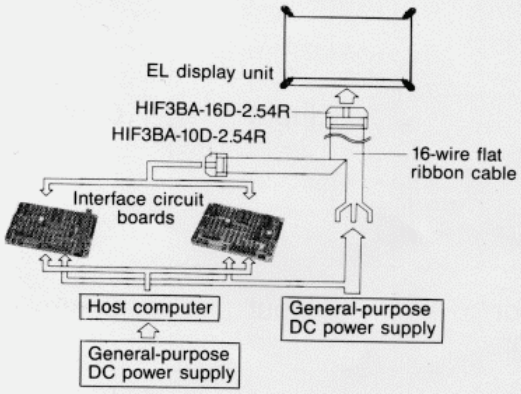


LJ232F02



Example of connection to EL display unit

1. Use a 16-wire flat ribbon cable for connecting the interface circuit boards to the EL display unit. Connect one end (16-pin socket) of the cable to the EL display unit. The other end of the cable should be divided into 10 wires and 6 wires. Connect the 10 wires to the interface circuit board and the 6 wires to the power supply. A 25V source voltage is applied to LJ720U22. Two wires of the 10-wire end of the cable should be used for 25V power supply when using LJ232F01.
2. Length of the flat ribbon cable should not exceed 50 cm to prevent induction noise to the EL display unit.
3. The interface circuit board contains a circuit for generating a synchronizing signal to be sent to the EL display unit. Its operation is controlled by incoming commands. DIP switches on the interface circuit board must be set properly depending on the model of the EL display unit and the equipment sending commands to the interface circuit board. (Refer to the technical literature for interface circuit board for details.)



■ Handling Precautions

1. The EL display unit must be handled with utmost care to prevent damage from static discharges. The assembler and every facility at the work site must be well grounded before handling the unit. Special attention must be used when handling a baseplate type EL display unit. Hold it by the mounting tabs provided at four corners of the panel.
2. The EL panel is made of glass. It will be easily broken if a strong shock is applied.
3. Do not attempt to remove or disassemble the display control board or SUMI card. Removal or disassembly may result in a failure of the unit. Do not touch any IC incorporated in the EL display unit. Static charge may cause a breakdown of the IC.

Operating Precautions

1. The EL display unit must be used in the rated voltage range and rated operating temperature range. It may fail if used outside the rated operating ranges. If it is assembled into equipment, due consideration must be taken in the design to provide sufficient air circulation and ventilation.
2. Even a small amount of condensation at the connector pins and circuits may cause malfunction. Do not operate the unit under condensing conditions, especially under high temperature and high humidity conditions.
3. Use 1.27 mm wire pitch flat ribbon cable (conductor type AWG # 28) or its equivalent as a signal and power supply cable.
4. Do not touch the display control board on the rear side of the display panel when it is operated. The board produces AC pulses of about 200V which present the risk of electric shock hazards.
5. When a fixed pattern is displayed on the panel for an extended period of time, luminance may vary significantly in the low luminance range.

LJ320U21

Features

- **Display format:** 320 (W) × 240 (H) dots
- **Dot pitch ratio:** 1:1
- **Input signal level:** LS TTL level
- **Drive method:** P-N symmetric drive
- **Structure:** Al frame
- **Net weight:** Approx. 600g

■ Absolute maximum ratings

(Ta=25°C)

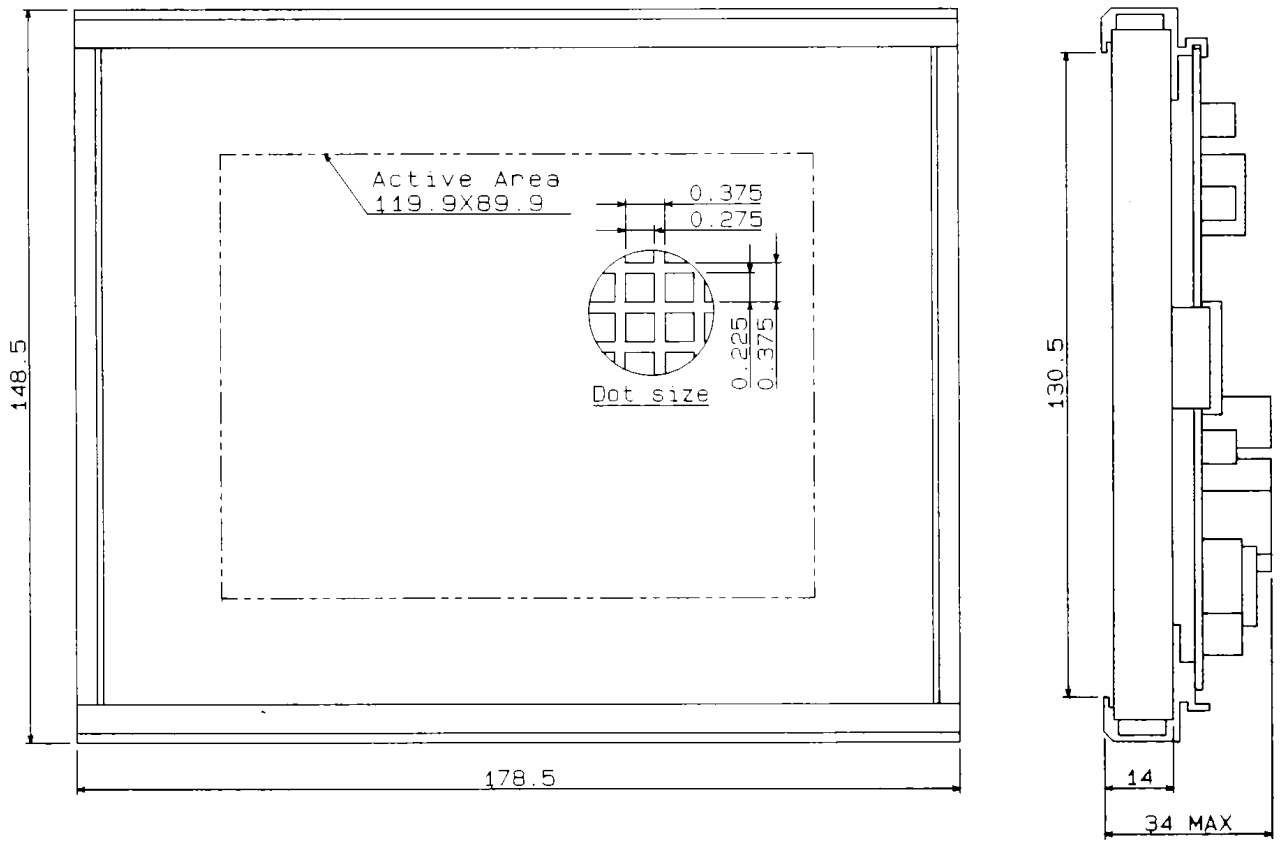
Parameter	Symbol	Rating	Unit
Interface signal (Logic "H")	V_{IH}	5.5	V
Interface signal (Logic "L")	V_{IL}	−0.5	V
Supply voltage (Logic)	V_L	7	V
Supply voltage (Panel drive)	V_D	18	V
Operating temperature	Topr	0 to +55	°C
Storage temperature	Tstg	−25 to +70	°C

■ Corresponding connector:

HIF3BA-16D-2.54R (HIROSE) or equivalents

Outline Dimensions

(Unit:mm)



Connector
HIF3F-16PA-2.54DS (HIROSE ELECTRIC) or equivalents.

Electro-optical Characteristics

(Ta=25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	V_L	—	4.75	5.0	5.25	V
Supply corrent (Logic)	I_L	V_L=5V	100	—	450	mA
Supply voltage (Panel drive)	V_D	—	14.25	15.0	15.75	V
Supply current (Panel drive)	I_D	V_D=15V	50	—	550	mA
Power consumption	P_T	V_L=5V, V_D=15V	—	8	—	W
Luminance	B_{ON}	All dots lit	20	—	—	fL
Off luminance	B_{OFF}	All dots turned off	—	—	1.0	fL
Luminance distribution	ΔB_{DIS}	All dots lit	—	—	35	%

Interface Signals

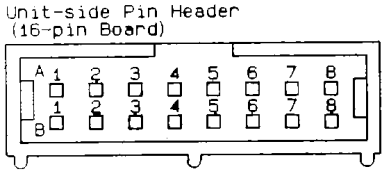
Pin No.	Symbol	Description
A-1	D_{IN}	Data signal
B-1	GND	Ground
A-2	CKD	Data transfer clock
B-2	GND	Ground
A-3	H.D	Horizontal sync. signal
B-3	GND	Ground
A-4	V.D	Vertical sync. signal
B-4	GND	Ground
A-5	GND	Ground
B-5	GND	Ground
A-6	GND	Ground
B-6	GND	Ground
A-7	V_L	+5V
B-7	V_L	+5V
A-8	V_D	+15V
B-8	V_D	+15V

Interface Timing Ratings

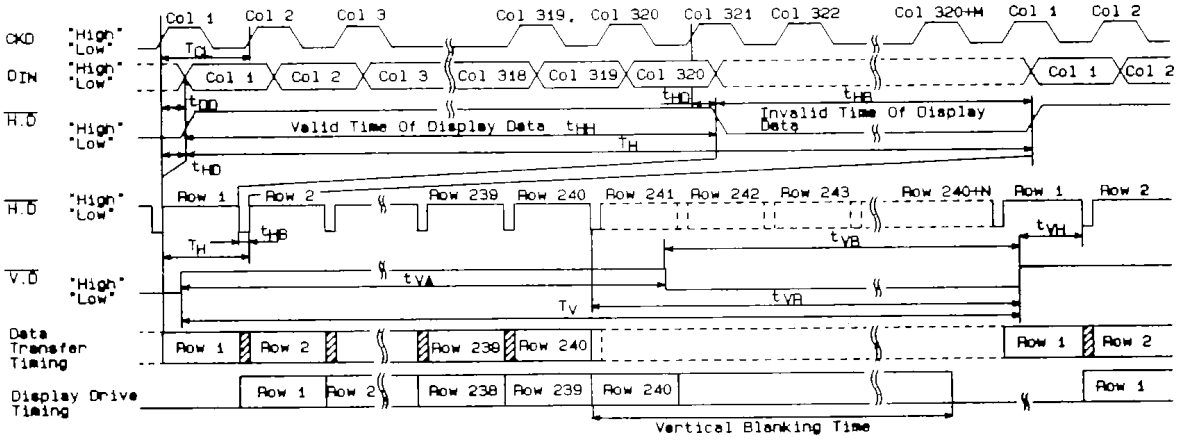
(Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	$1/T_{CL}$	4.4	—	7.5	MHz
Clock duty	$T_{CL}(H)/T_{CL}\times 100$	45	—	55	%
Horizontal sync. signal cycle time	T_H	62	—	75	μsec
Horizontal sync. signal blanking time	t_{HB}	2	—	—	μsec
Vertical sync. signal blanking time	t_{VB}	1	—	$N\times T_H$	μsec
Vertical sync. signal valid time	t_{VA}	$240\times T_H$	—	—	μsec
Frame frequency	$1/T_V$	50	60	63	Hz
Data signal delay time required	t_{DD}	0.01	—	T_{CL}	μsec
Horizontal sync. signal delay time required	t_{HD}	0.01	—	$T_{CL}/2$	μsec
Vertical sync. signal rise wait time	t_{VR}	4×62	—	—	μsec
Vertical sync. rise timing	t_{VH}	62	—	$T_H-t_{HB}+50$	μsec

Connector



Interface Timing Chart



LJ320U27

Features

- **Display format:** 320 (W) × 256 (H) dots
- **Dot pitch ratio:** 1:1
- **Input signal level:** LS TTL level
- **Drive method:** P-P symmetric drive
- **Structure:** Baseplate
- **Net weight:** Approx. 400g
- **LJ320U26:** +5V, +15V type is also available.

Absolute maximum ratings

(Ta=25°C)

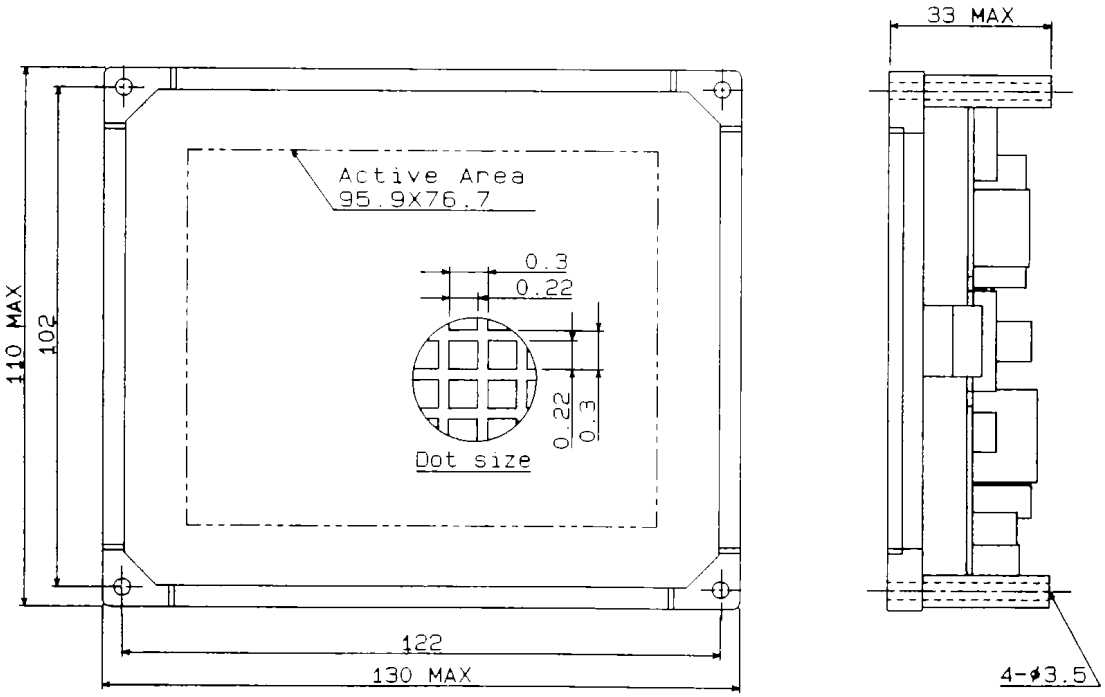
Parameter	Symbol	Rating	Unit
Interface signal (Logic "H")	V_{IH}	5.5	V
Interface signal (Logic "L")	V_{IL}	−0.5	V
Supply voltage (Logic)	V_L	7	V
Supply voltage (Panel drive)	V_D	14	V
Operating temperature	Topr	−5 to +65	°C
Storage temperature	Tstg	−40 to +80	°C

Corresponding connector:

HIF3A-16D-2.54R (HIROSE) or equivalents

Outline Dimensions

(Unit:mm)



Connector
HIF3F-16PA-2.54DSA (HIROSE ELECTRIC) or equivalents.

Electro-optical Characteristics

(Ta=25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	V_L		4.75	5.0	5.25	V
Supply current (Logic)	I_L	V_L=5V	(50)	—	(450)	mA
Supply voltage (Panel drive)	V_D		11.4	12.0	12.6	V
Supply current (Panel drive)	I_D	V_D=15V	(100)	—	(550)	mA
Power consumption	P_T	V_L=5V, V_D=15V	—	(5)	—	W
Luminance	B_{ON}	All dots lit	23	30	—	fL
Off luminance	B_{OFF}	All dots turned off	—	—	1.0	fL
Luminance distribution	ΔB_{DIS}	All dots lit	—	—	35	%

( ): Tentative

Interface Signals

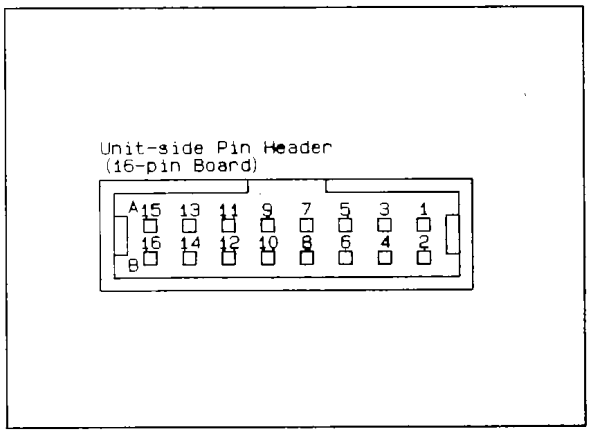
Pin No.	Symbol	Description
1	V_D	+12V
2	V_D	+12V
3	V_L	+5V
4	V_L	+5V
5	GND	Ground
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	V.D	Vertical sync. signal
10	GND	Ground
11	H.D	Horizontal sync. signal
12	GND	Ground
13	CKD	Data transfer clock
14	GND	Ground
15	D_{IN}	Data signal
16	GND	Ground

Interface Timing Ratings

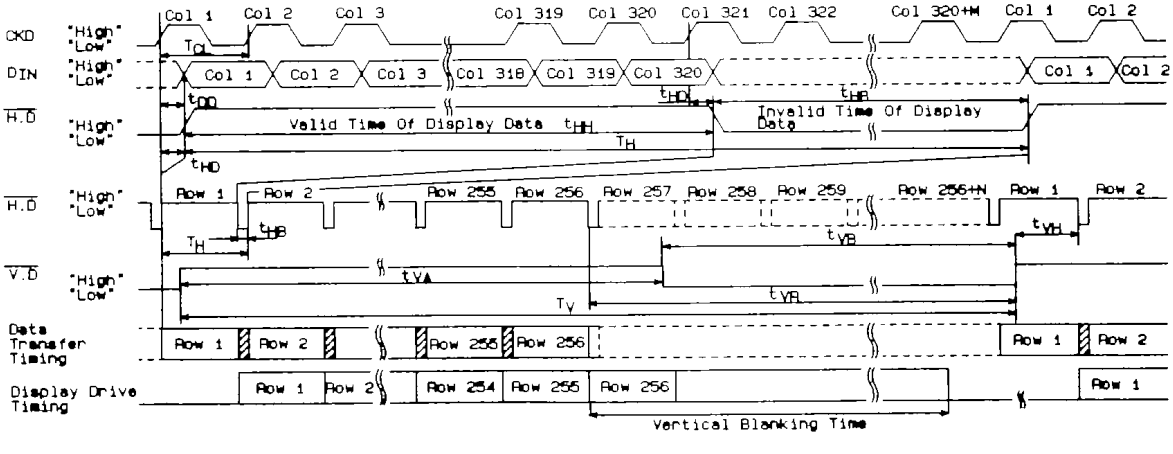
(Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	$1/T_{CL}$	4.4	—	16	MHz
Clock duty	$T_{CL}(H)/T_{CL}\times 100$	45	—	55	%
Horizontal sync. signal cycle time	T_H	60	—	75	μsec
Horizontal sync. signal blanking time	t_{HB}	2	—	—	μsec
Vertical sync. signal blanking time	t_{VB}	1	—	$N\times T_H$	μsec
Vertical sync. signal valid time	t_{VA}	$256\times T_H$	—	—	μsec
Frame frequency	$1/T_V$	50	60	63	Hz
Data signal delay time required	t_{DD}	0.01	—	T_{CL}	μsec
Horizontal sync. signal delay time required	t_{HD}	0.01	—	$T_{CL}/2$	μsec
Vertical sync. signal rise wait time	t_{VR}	4×60	—	—	μsec
Vertical sync. rise timing	t_{VH}	60	—	$T_H-t_{HB}+50$	μsec

Connector



Interface Timing Chart



LJ512U21

Features

- **Display format:** 512 (W) × 128 (H) dots
- **Dot pitch ratio:** 1:1
- **Input signal level:** LS TTL level
- **Drive method:** P-N symmetric drive
- **Structure:** Al frame
- **Net weight:** Approx. 600g

Absolute maximum ratings

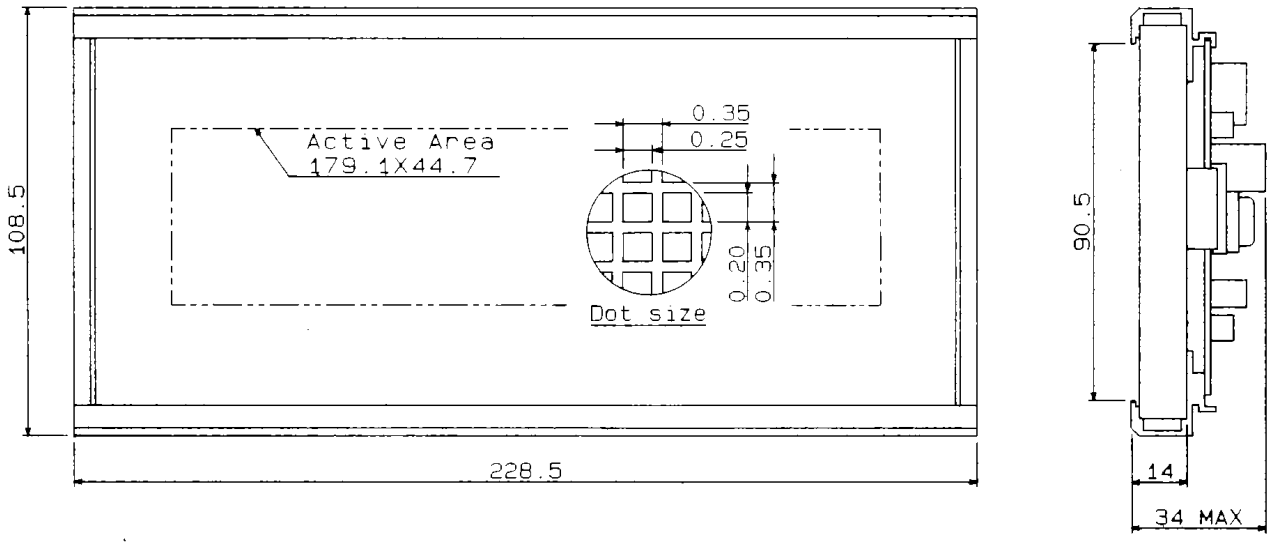
(Ta=25°C)

Parameter	Symbol	Rating	Unit
Interface signal (Logic "H")	V_{iH}	5.5	V
Interface signal (Logic "L")	V_{iL}	−0.5	V
Supply voltage (Logic)	V_L	7	V
Supply voltage (Panel drive)	V_D	18	V
Operating temperature	Topr	0 to +55	°C
Storage temperature	Tstg	−25 to +70	°C

- **Corresponding connector:**
  HIF3BA-16D-2.54R (HIROSE) or equivalents

Outline Dimensions

(Unit:mm)



Connector
HIF3F-16PA-2.54DS (HIROSE ELECTRIC) or equivalents.

Electro-optical Characteristics

(Ta=25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	V_L	—	4.75	5.0	5.25	V
Supply current (Logic)	I_L	V_L=5V	100	—	450	mA
Supply voltage (Panel drive)	V_D	—	14.25	15.0	15.75	V
Supply current (Panel drive)	I_D	V_D=15V	50	—	350	mA
Power consumption	P_T	V_L=5V, V_D=15V	—	6	—	W
Luminance	B_{ON}	All dots lit	25	—	—	fL
Off luminance	B_{OFF}	All dots turned off	—	—	1.0	fL
Luminance distribution	$\triangle B_{DIS}$	All dots lit	—	—	35	%

Interface Signals

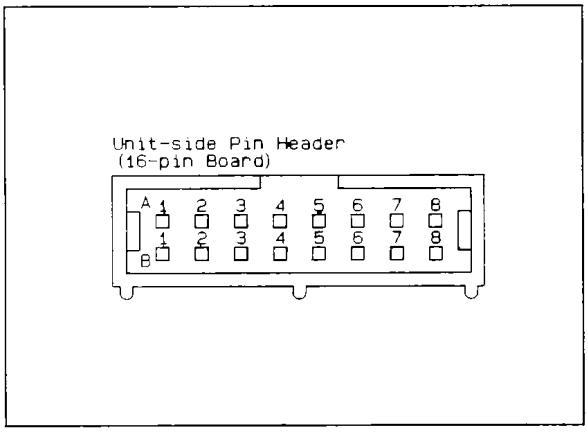
Pin No.	Symbol	Description
A-1	D_{IN}	Data signal
B-1	GND	Ground
A-2	CKD	Data transfer clock
B-2	GND	Ground
A-3	H.D	Horizontal sync. signal
B-3	GND	Ground
A-4	V.D	Vertical sync. signal
B-4	GND	Ground
A-5	GND	Ground
B-5	GND	Ground
A-6	GND	Ground
B-6	GND	Ground
A-7	V_L	+5V
B-7	V_L	+5V
A-8	V_D	+15V
B-8	V_D	+15V

Interface Timing Ratings

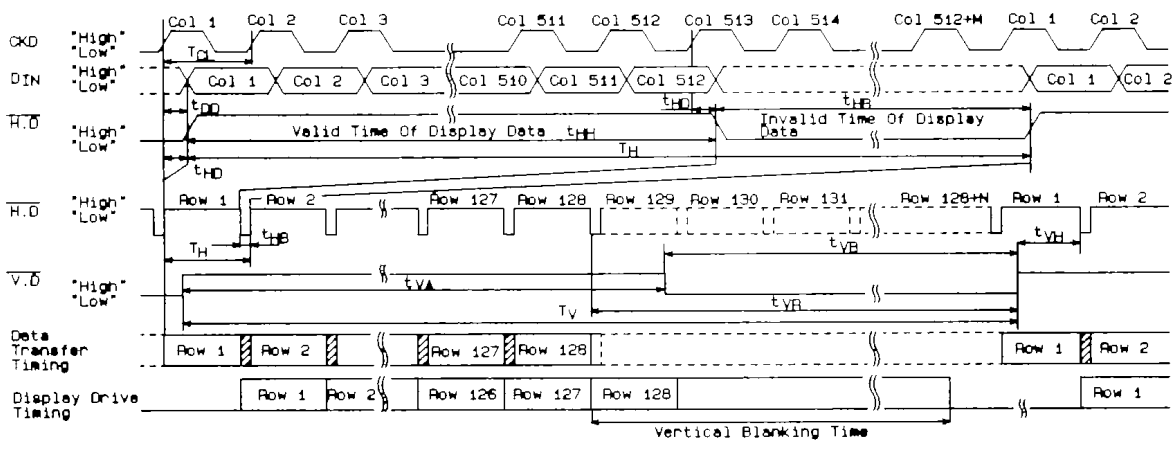
(Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	$1/T_{CL}$	4.8	—	7.5	MHz
Clock duty	$T_{CL}(H)/T_{CL}\times 100$	45	—	55	%
Horizontal sync. signal cycle time	T_H	84	—	110	μsec
Horizontal sync. signal blanking time	t_{HB}	2	—	—	μsec
Vertical sync. signal blanking time	t_{VB}	1	—	$N\times T_H$	μsec
Vertical sync. signal valid time	t_{VA}	$128\times T_H$	—	—	μsec
Frame frequency	$1/T_V$	50	70	82	Hz
Data signal delay time required	t_{DD}	0.01	—	T_{CL}	μsec
Horizontal sync. signal delay time required	t_{HD}	0.01	—	$T_{CL}/2$	μsec
Vertical sync. signal rise wait time	t_{VR}	4×84	—	—	μsec
Vertical sync. rise timing	t_{VH}	84	—	$T_H-t_{HB}+50$	μsec

Connector



Interface Timing Chart



LJ512U32

Features

- **Display format:** 512 (W) × 256 (H) dots
- **Dot pitch ratio:** 1:1
- **Input signal level:** LS TTL level
- **Drive method:** P-P symmetric drive
- **Structure:** Baseplate
- Detachable DC/DC converter
- **Net weight:** Approx. 480g (540g*)
  * Including DC/DC converter
- **LJ51AU27:** +5V, +15V type is also available.
  LJ512U27: Al frame type is also available.

Absolute maximum ratings

(Ta=25°C)

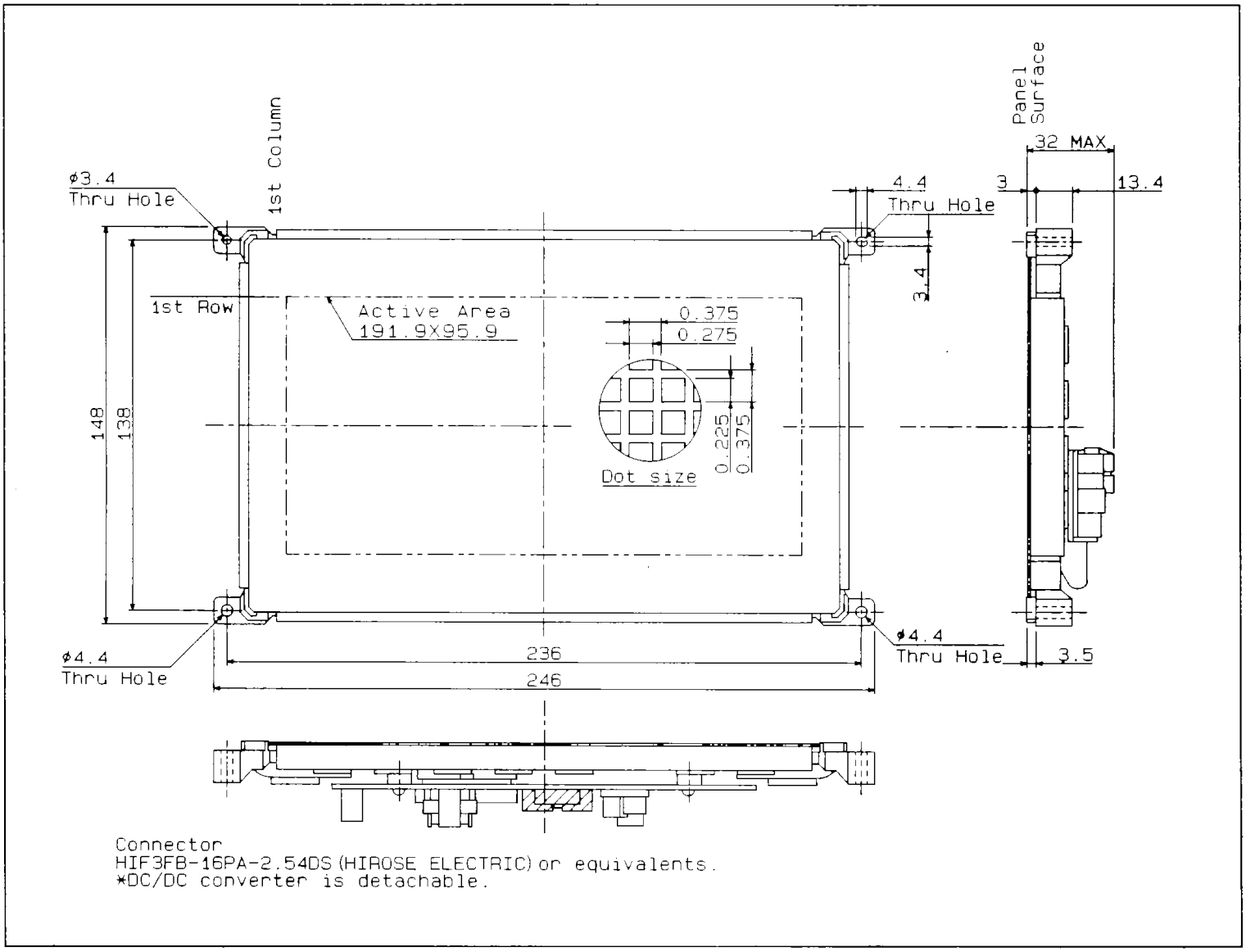
Parameter	Symbol	Rating	Unit
Interface signal (Logic "H")	V_{IH}	5.5	V
Interface signal (Logic "L")	V_{IL}	−0.5	V
Supply voltage (Logic)	V_L	7	V
Supply voltage (Panel drive)	V_D	14	V
Operating temperature	Topr	−5 to +55	°C
Storage temperature	Tstg	−40 to +80	°C

Corresponding connector:

HIF3BA-16D-2.54R (HIROSE) or equivalents

Outline Dimensions

(Unit:mm)



Electro-optical Characteristics

(Ta=25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	V_L		4.75	5.0	5.25	V
Supply current (Logic)	I_L	V_L=5V	100	—	500	mA
Supply voltage (Panel drive)	V_D		11.4	12.0	12.6	V
Supply current (Panel drive)	I_D	V_D=12V	40	—	750	mA
Power consumption	P_T	V_L=5V, V_D=12V	—	7	—	W
Luminance	B_{ON}	All dots lit	23	34	—	fL
Off luminance	B_{OFF}	All dots turned off	—	—	1.0	fL
Luminance distribution	$\triangle B_{DIS}$	All dots lit	—	—	30	%

Interface Signals

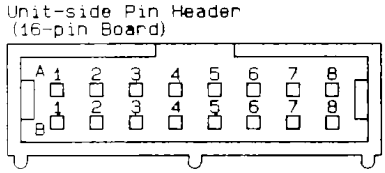
Pin No.	Symbol	Description
A-1	$D_{IN}0$	Data signal for odd column
B-1	$D_{IN}1$	Data signal for even column
A-2	CKD	Data transfer clock
B-2	GND	Ground
A-3	H.D	Horizontal sync. signal
B-3	GND	Ground
A-4	V.D	Vertical sync. signal
B-4	N.C	—
A-5	GND	Ground
B-5	GND	Ground
A-6	N.C	—
B-6	N.C	—
A-7	V_L	+5V
B-7	V_L	+5V
A-8	V_D	+12V
B-8	V_D	+12V

Interface Timing Ratings

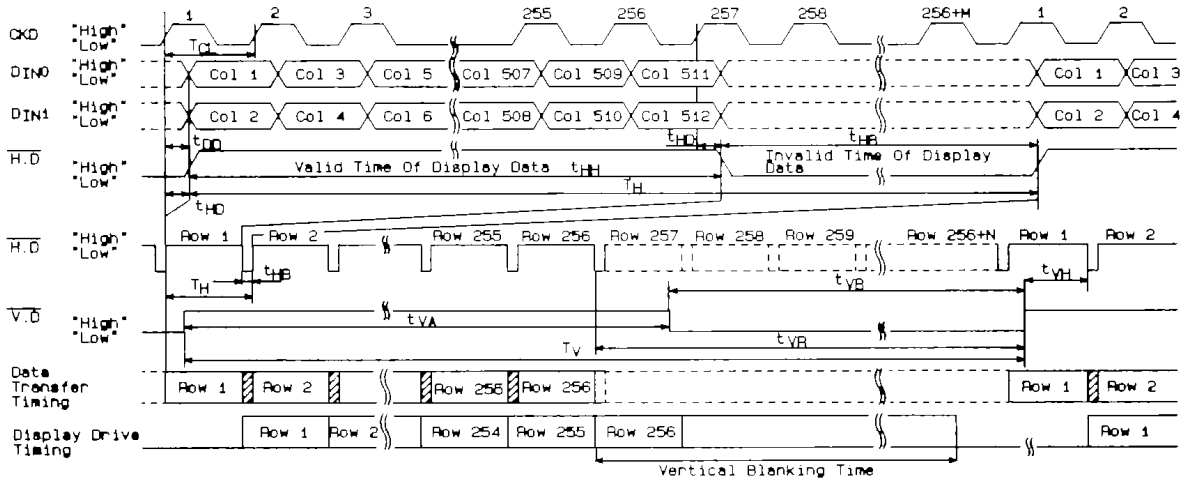
(Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	$1/T_{CL}$	3.9	—	8	MHz
Clock duty	$T_{CL}(H)/T_{CL}\times 100$	45	—	55	%
Horizontal sync. signal cycle time	T_H	60	—	69	μsec
Horizontal sync. signal blanking time	t_{HB}	2	—	—	μsec
Vertical sync. signal blanking time	t_{VB}	1	—	$N\times T_H$	μsec
Vertical sync. signal valid time	t_{VA}	$256\times T_H$	—	—	μsec
Frame frequency	$1/T_V$	55	60	62	Hz
Data signal delay time required	t_{DD}	0.01	—	T_{CL}	μsec
Horizontal sync. signal delay time required	t_{HD}	0.01	—	$T_{CL}/2$	μsec
Vertical sync. signal rise wait time	t_{VR}	4×60	—	—	μsec
Vertical sync. rise timing	t_{VH}	60	—	$T_H-t_{HB}+50$	μsec

Connector



Interface Timing Chart



LJ640U23 Series

LJ640U23 LJ640U24
LJ640U25 LJ640U30

Features

- **Display format:** 640 (W) × 200 (H) dots
- **Dot pitch ratio:**
  1:1 ··· LJ640U25 1:1.4 ··· LJ640U23
  1:1.6 ··· LJ640U30 1:2 ··· LJ640U24
- **Input signal level:** LS TTL level
- **Drive method:** P-P symmetric drive
- **Structure:** Al frame (LJ640U23/24/30)
  Baseplate (LJ640U25)
- **Net weight:** Approx. 600g (LJ640U25)
  Approx. 650g (LJ640U23/30)
  Approx. 750g (LJ640U24)
- **LJ640U80:** Extended temperature type is also available.
  (Dot pitch ratio 1:1)
  LJ640U21: Al frame type is also available.
  (Dot pitch ratio 1:1, +5V, +15V)

■ Absolute maximum ratings

(Ta=25°C)

Parameter	Symbol	Rating	Unit
Interface signal (Logic "H")	V_{IH}	5.5	V
Interface signal (Logic "L")	V_{IL}	−0.5	V
Supply voltage (Logic)	V_L	7	V
Supply voltage (Panel drive)	V_D	18(14)	V
Operating temperature	Topr	0(−5) to +55	°C
Storage temperature	Tstg	−25 to +70	°C

Note) ( ): LJ640U25

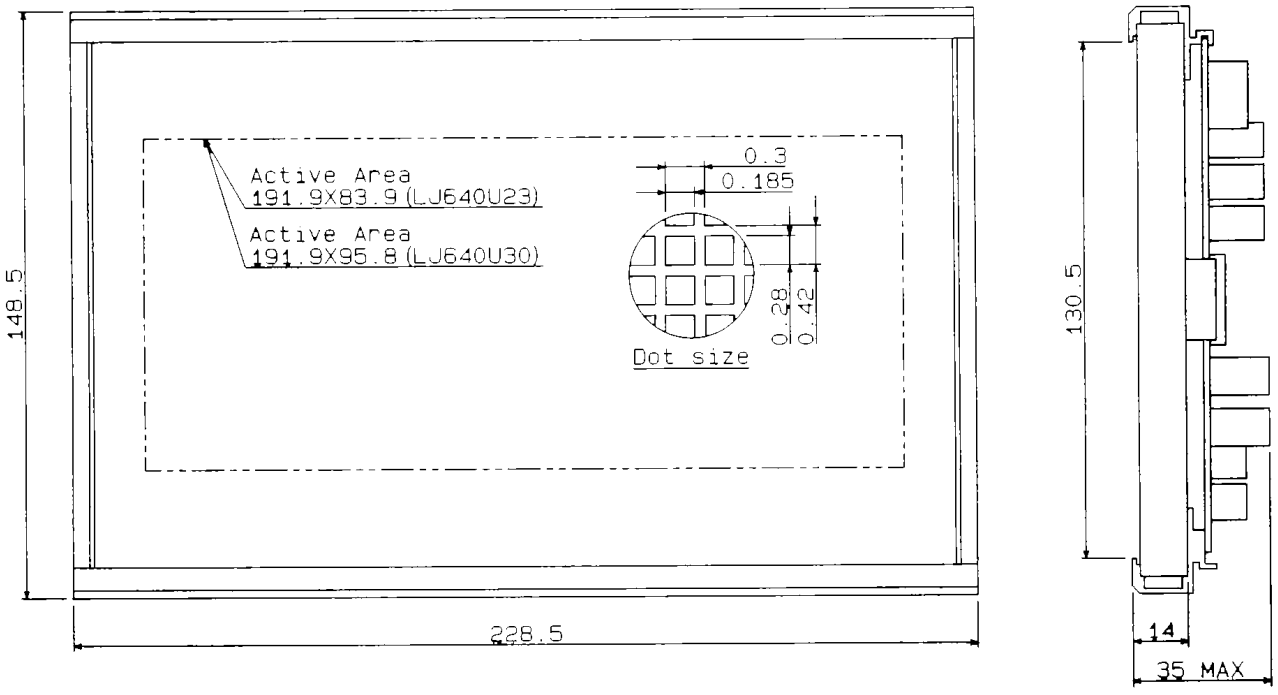
■ Corresponding connector:

HIF3BA-16D-2.54R (HIROSE) or equivalents

Outline Dimensions

(Unit:mm)

LJ640U23/LJ640U30

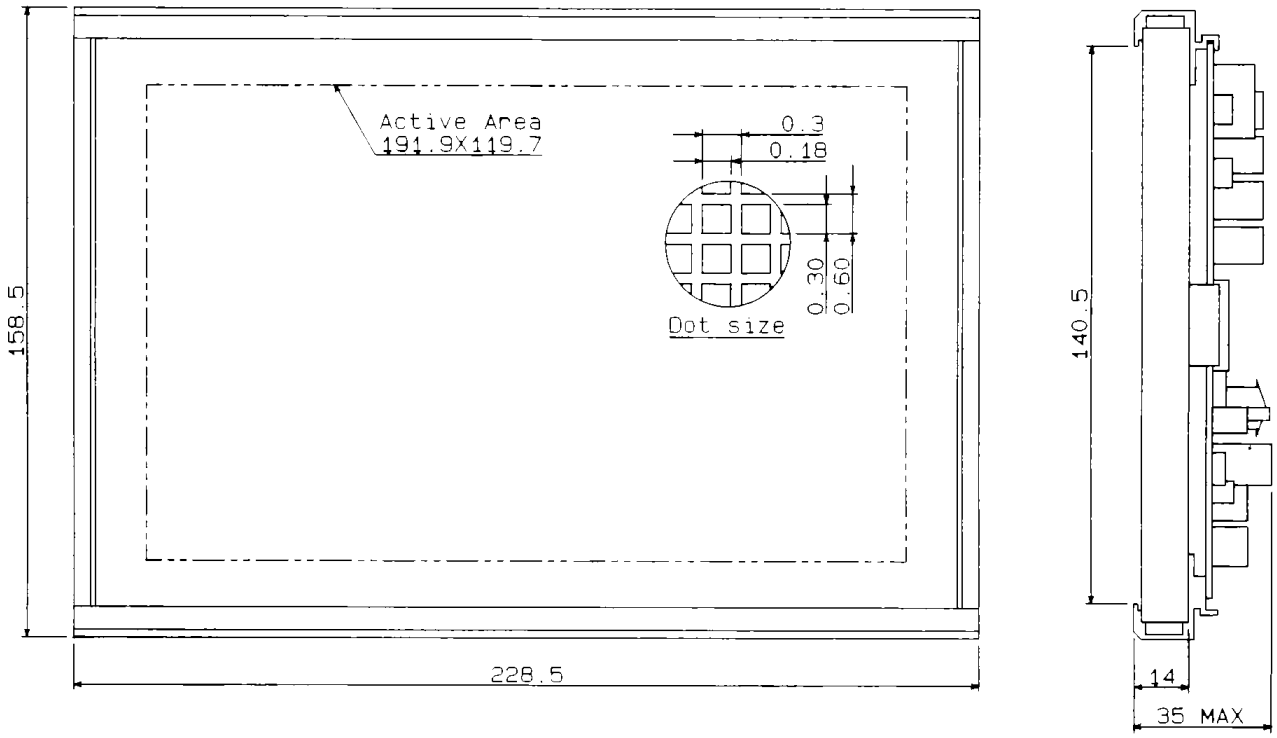


Connector
HIF3FB-16PA-2.54DS (HIROSE ELECTRIC) or equivalents.

Outline Dimensions

(Unit:mm)

LJ640U24

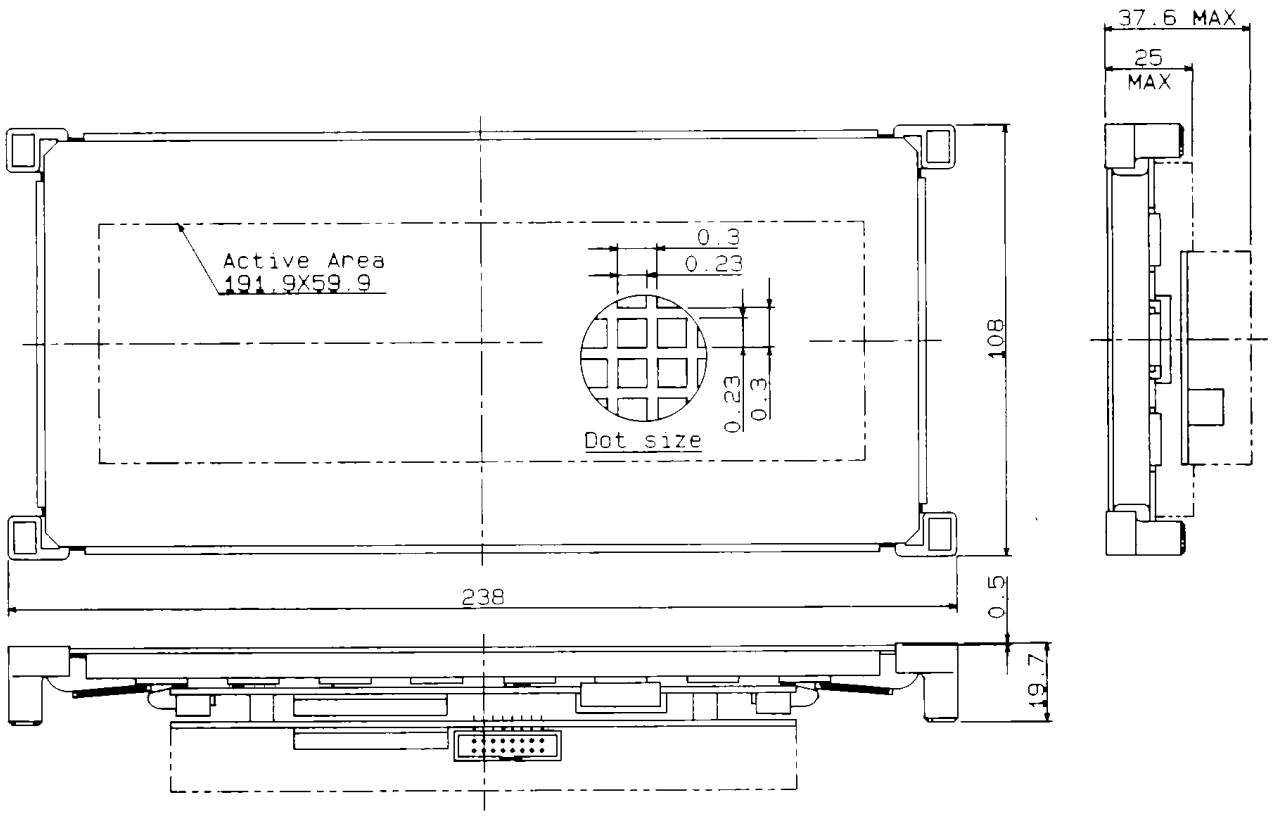


Connector
HIF3FB-16PA-2.54DS(HIROSE ELECTRIC) or equivalents.

Outline Dimentions

(Unit: mm)

LJ640U25



Connector
HIF3FB-16PA-2.54DS (HIROSE ELECTRIC) or equivalents.

LJ640U23/LJ640U24/LJ640U25/LJ640U30

Electro-optical Characteristics

(Ta=25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	V_L	—	4.75	5.0	5.25	V
Supply current (Logic)	I_L	V_L=5V	100	—	450(500)	mA
Supply voltage (Panel drive)	V_D	—	14.25 (11.4)	15.0 (12.0)	15.75 (12.6)	V
Supply current (Panel drive)	I_D	V_D=15V(12V)	50(100)	—	750{800}	mA
Power consumption	P_T	V_L=5V, V_D=15V(12V)	—	10	—	W
Luminance	B_{ON}	All dots lit	20(23)	30(34)	—	fL
Off luminance	B_{OFF}	All dots turned off	—	—	1.0	fL
Luminance distribution	$\triangle B_{DIS}$	All dots lit	—	—	35	%

Note) ( ): LJ640U25
{ }: LJ640U24

Interface Signals

Pin No.	Symbol	Description
A-1	D_{IN}	Data signal
B-1	GND	Ground
A-2	CKD	Data transfer clock
B-2	GND	Ground
A-3	H.D	Horizontal sync. signal
B-3	GND	Ground
A-4	V.D	Vertical sync. signal
B-4	GND	Ground
A-5	GND	Ground
B-5	GND	Ground
A-6	GND	Ground
B-6	GND	Ground
A-7	V_L	+5V
B-7	V_L	+5V
A-8	V_D	+15V(+12V*)
B-8	V_D	+15V(+12V*)

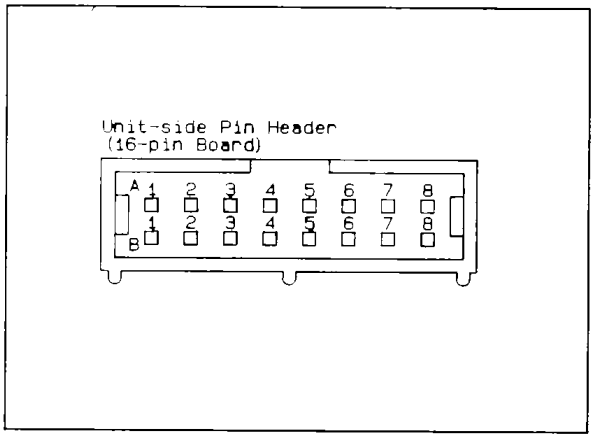
*LJ640U25:12V

Interface Timing Ratings

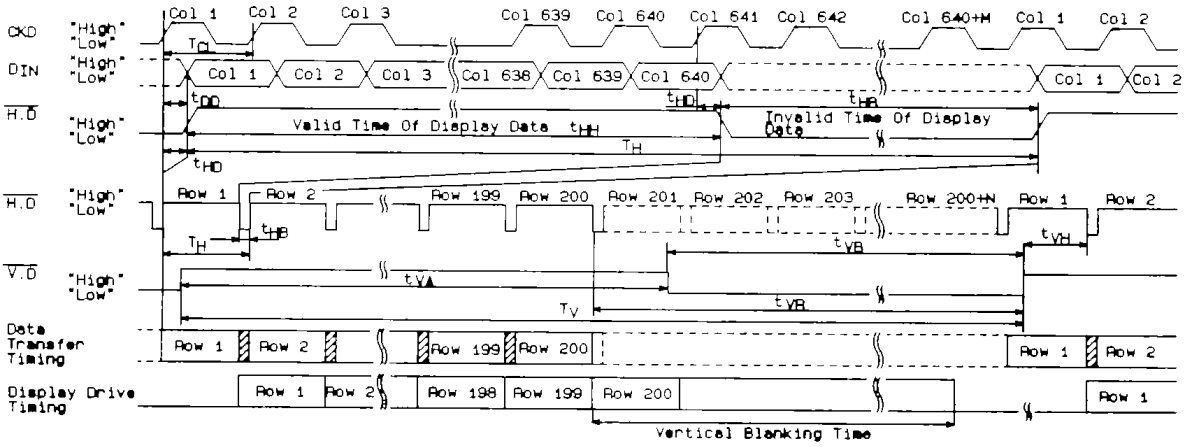
(Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	$1/T_{CL}$	8.8	—	16	MHz
Clock duty	$T_{CL}(H)/T_{CL}\times 100$	45	—	55	%
Horizontal sync. signal cycle time	T_H	60	—	75	μsec
Horizontal sync. signal blanking time	t_{HB}	2	—	—	μsec
Vertical sync. signal blanking time	t_{VB}	1	—	$N\times T_H$	μsec
Vertical sync. signal valid time	t_{VA}	$200\times T_H$	—	—	μsec
Frame frequency	$1/T_V$	50	60	64	Hz
Data signal delay time required	t_{DD}	0.01	—	T_{CL}	μsec
Horizontal sync. signal delay time required	t_{HD}	0.01	—	$T_{CL}/2$	μsec
Vertical sync. signal rise wait time	t_{VR}	4×60	—	—	μsec
Vertical sync. rise timing	t_{VH}	60	—	$T_H-t_{HB}+50$	μsec

Connector



Interface Timing Chart



LJ640U32

Features

- **Display format:** 640 (W) × 400 (H) dots
- **Dot pitch ratio:** 1:1
- **Input signal level:** LS TTL level
- **Drive method:** P-P symmetric drive
- **Structure:** Baseplate
- Detachable DC/DC converter
- **Net weight:** Approx. 480g (540g*)
  *Including DC/DC converter
- **LJ640U31:** +5V, +24V type is also available.
  LJ640U27: Al frame type is also available.

■ Absolute maximum ratings

(Ta=25°C)

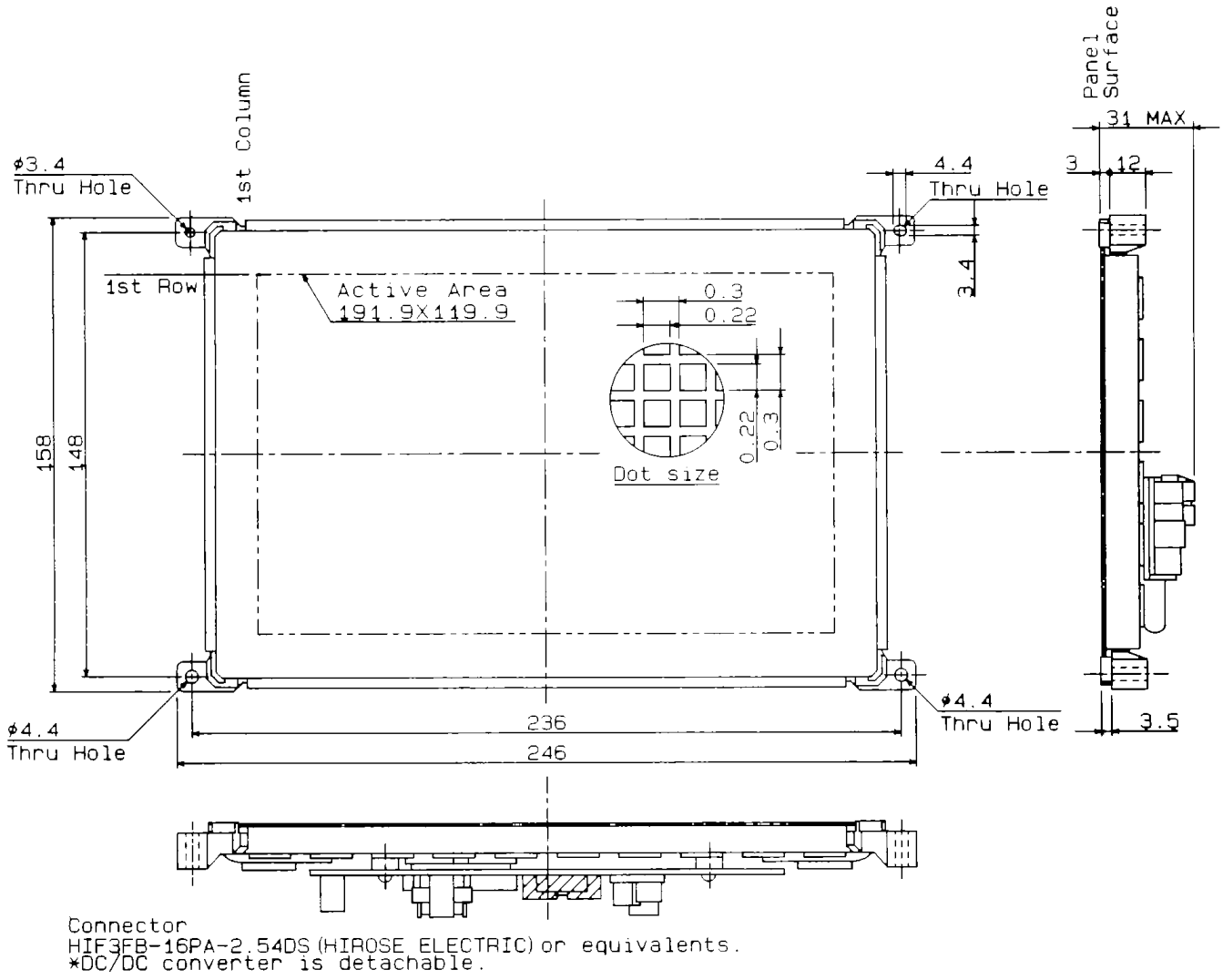
Parameter	Symbol	Rating	Unit
Interface signal (Logic "H")	V_{IH}	5.5	V
Interface signal (Logic "L")	V_{IL}	−0.5	V
Supply voltage (Logic)	V_L	7	V
Supply voltage (Panel drive)	V_D	14	V
Operating temperature	Topr	−5 to +55	°C
Storage temperature	Tstg	−40 to +80	°C

■ Corresponding connector:

HIF3BA-16D-2.54R (HIROSE) or equivalents

Outline Dimensions

(Unit:mm)



Electro-optical Characteristics

(Ta=25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	V_L	—	4.75	5.0	5.25	V
Supply current (Logic)	I_L	V_L=5V	100	—	700	mA
Supply voltage (Panel drive)	V_D	—	11.4	12.0	12.6	V
Supply current (Panel drive)	I_D	V_D=12V	40	—	1350	mA
Power consumption	P_T	V_L=5V, V_D=12V	—	11	—	W
Luminance	B_{ON}	All dots lit	23	34	—	fL
Off luminance	B_{OFF}	All dots turned off	—	—	1.0	fL
Luminance distribution	$\triangle B_{DIS}$	All dots lit	—	—	30	%

Interface Signals

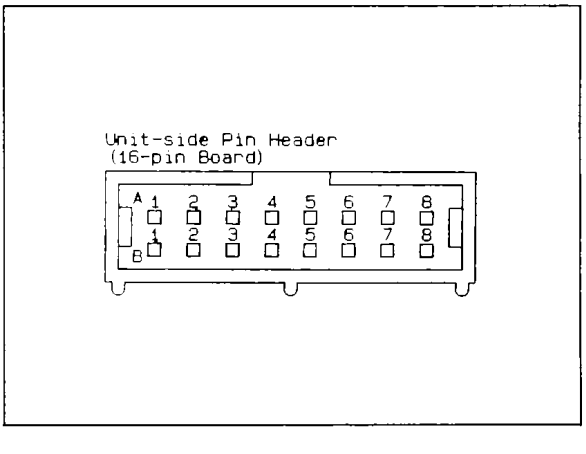
Pin No.	Symbol	Description
A-1	$D_{IN}0$	Data signal for odd column
B-1	$D_{IN}1$	Data signal for even column
A-2	CKD	Data transfer clock
B-2	GND	Ground
A-3	H.D	Horizontal sync. signal
B-3	GND	Ground
A-4	V.D	Vertical sync. signal
B-4	NC	—
A-5	GND	Ground
B-5	GND	Ground
A-6	NC	—
B-6	NC	—
A-7	V_L	+5V
B-7	V_L	+5V
A-8	V_D	+12V
B-8	V_D	+12V

Interface Timing Ratings

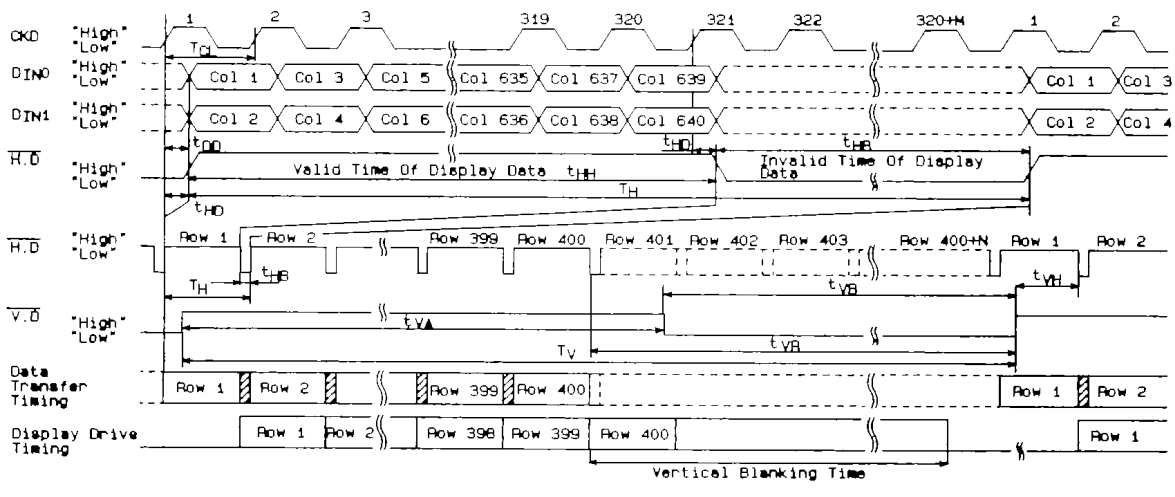
(Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	$1/T_{CL}$	7.5	—	11.0	MHz
Clock duty	$T_{CL}(H)/T_{CL}\times 100$	45	—	55	%
Horizontal sync. signal cycle time	T_H	40	—	45	μsec
Horizontal sync. signal blanking time	t_{HB}	2	—	—	μsec
Vertical sync. signal blanking time	t_{VB}	1	—	$N\times T_H$	μsec
Vertical sync. signal valid time	t_{VA}	$400\times T_H$	—	—	μsec
Frame frequency	$1/T_V$	55	60	62	Hz
Data signal delay time required	t_{DD}	0.01	—	T_{CL}	μsec
Horizontal sync. signal delay time required	t_{HD}	0.01	—	$T_{CL}/2$	μsec
Vertical sync. signal rise wait time	t_{VR}	4×40	—	—	μsec
Vertical sync. rise timing	t_{VH}	40	—	$T_H-t_{HB}+35$	μsec

Connector



Interface Timing Chart



LJ64ZU31

Features

- **Display format:** 640 (W) × 400 (H) dots
- **Dot pitch ratio:** 1:1
- 16-level gray scale
- **Input signal level:** LS TTL level
- **Drive method:** PWM symmetric drive
- **Structure:** Baseplate
- Detachable DC/DC converter
- **Net weight:** Approx. 535g (600g*)
  *Including DC/DC converter

Absolute maximum ratings

(Ta=25°C)

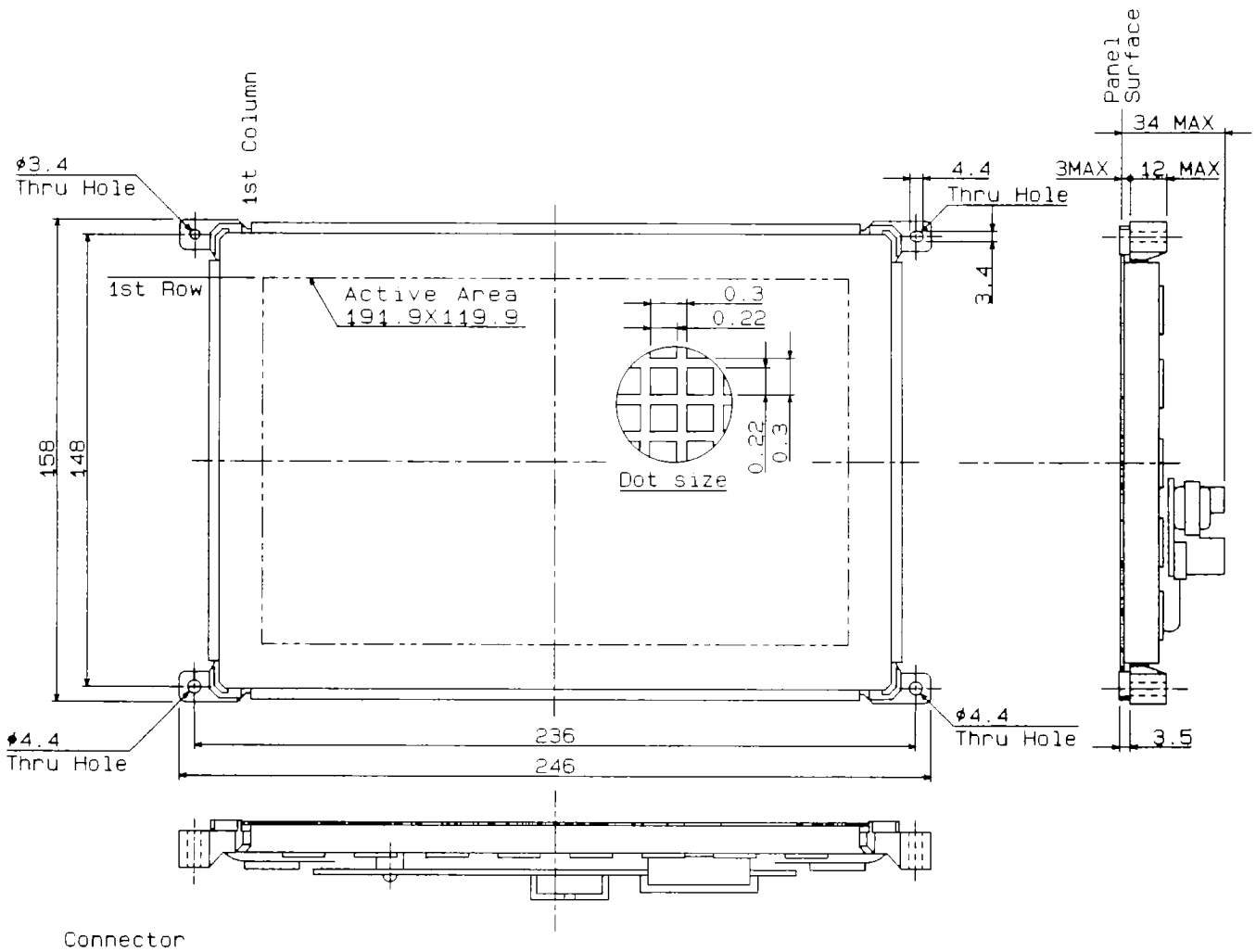
Parameter	Symbol	Rating	Unit
Interface signal (Logic "H")	V_{IH}	5.5	V
Interface signal (Logic "L")	V_{IL}	−0.5	V
Supply voltage (Logic)	V_L	7	V
Supply voltage (Panel drive)	V_D	27	V
Operating temperature	Topr	−5 to +55	°C
Storage temperature	Tstg	−40 to +80	°C

Corresponding connector:

HIF3BA-20D-2.54R (HIROSE) or equivalents

Outline Dimensions

(Unit:mm)



Connector
HIF3FC-20PA-2.54DS (HIROSE ELECTRIC) or equivalents.
*DC/DC converter is detachable.

Electro-optical Characteristics

(Ta=25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	V_L	—	4.75	5.0	5.25	V
Supply current (Logic)	I_L	V_L=5V	100	—	300	mA
Supply voltage (Panel drive)	V_D	—	22.8	24.0	25.2	V
Supply current (Panel drive)	I_D	V_D=24V	400	—	1000	mA
Power consumption	P_T	V_L=5V, V_D=24V	—	18	—	W
Luminance	B_{ON}	All dots lit	23	30	—	fL
Off luminance	B_{OFF}	All dots turned off	—	—	1.0	fL
Lumiance distribution	ΔB_{DIS}	All dots lit	—	—	35	%

Interface Signals

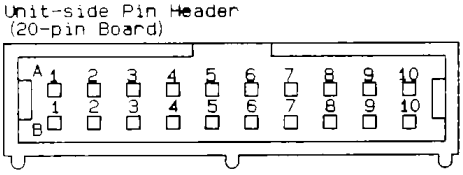
Pin No.	Symbol	Description
A-1	D1	Data signal
B-1	D0	
A-2	D3	
B-2	D2	
A-3	N.C	—
B-3	N.C	—
A-4	CKD	Data transfer clock
B-4	GND	Ground
A-5	H.D	Horizontal sync. signal
B-5	GND	Ground
A-6	V.D	Vertical sync. signal
B-6	GND	Ground
A-7	GND	Ground
B-7	GND	Ground
A-8	V_D	+24V
B-8	V_D	+24V
A-9	V_L	+5V
B-9	V_L	+5V
A-10	N.C	—
B-10	N.C	—

Interface Timing Ratings

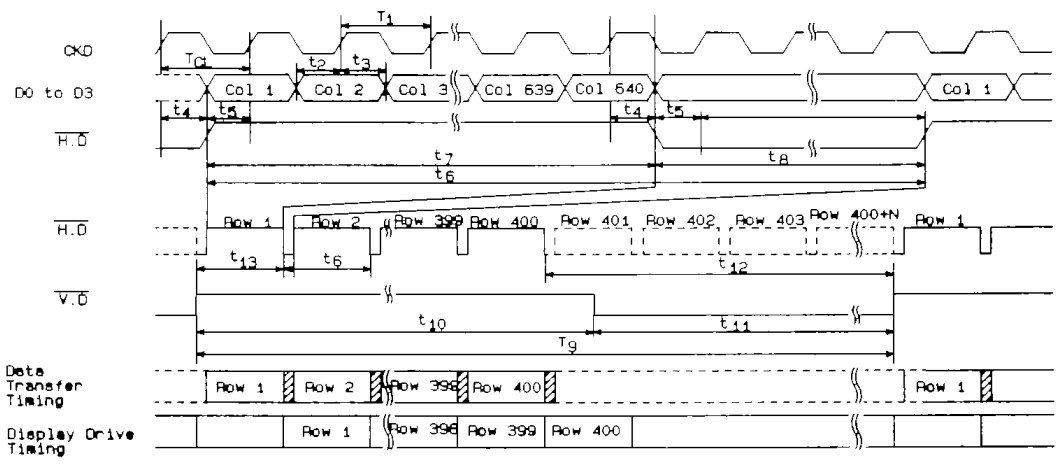
(Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	1/t1	13.5	—	22.0	MHz
Clock duty	t1(H)/t1 × 100	45	—	55	%
Data setup time	t2	10	—	—	nsec
Data hold time	t3	10	—	—	nsec
H.D hold time	t4	10	—	—	nsec
H.D setup time	t5	10	—	—	nsec
Horizontal sync. signal cycle time	t6	40	—	49	μsec
Horizontal sync. signal valid time (Valid time of display data)	t7		640 × t1		μsec
Horizontal sync. signal blanking time (Invalid time of display data)	t8	1	—	—	μsec
Frame frequency	1/t9	50	60	62	Hz
Vertical sync. signal valid time	t10	t6	400 × t6	—	μsec
Vertical sync. signal blanking time	t11	1	—	t9 − t6	μsec
Vertical sync. signal rise wait time	t12	4 × 40	—	—	μsec
Vertical sync. rise timing	t13	40	—	t7+35	μsec

Connector



Interface Timing Chart



LJ640U48

Features

- **Display format:** 640 (W) × 480 (H) dots
- **Dot pitch ratio:** 1:1
- **Input signal level:** LS TTL level
- **Drive method:** P-P symmetric drive
- **Structure:** Baseplate
- **Net weight:** Approx. 700g

Absolute maximum ratings

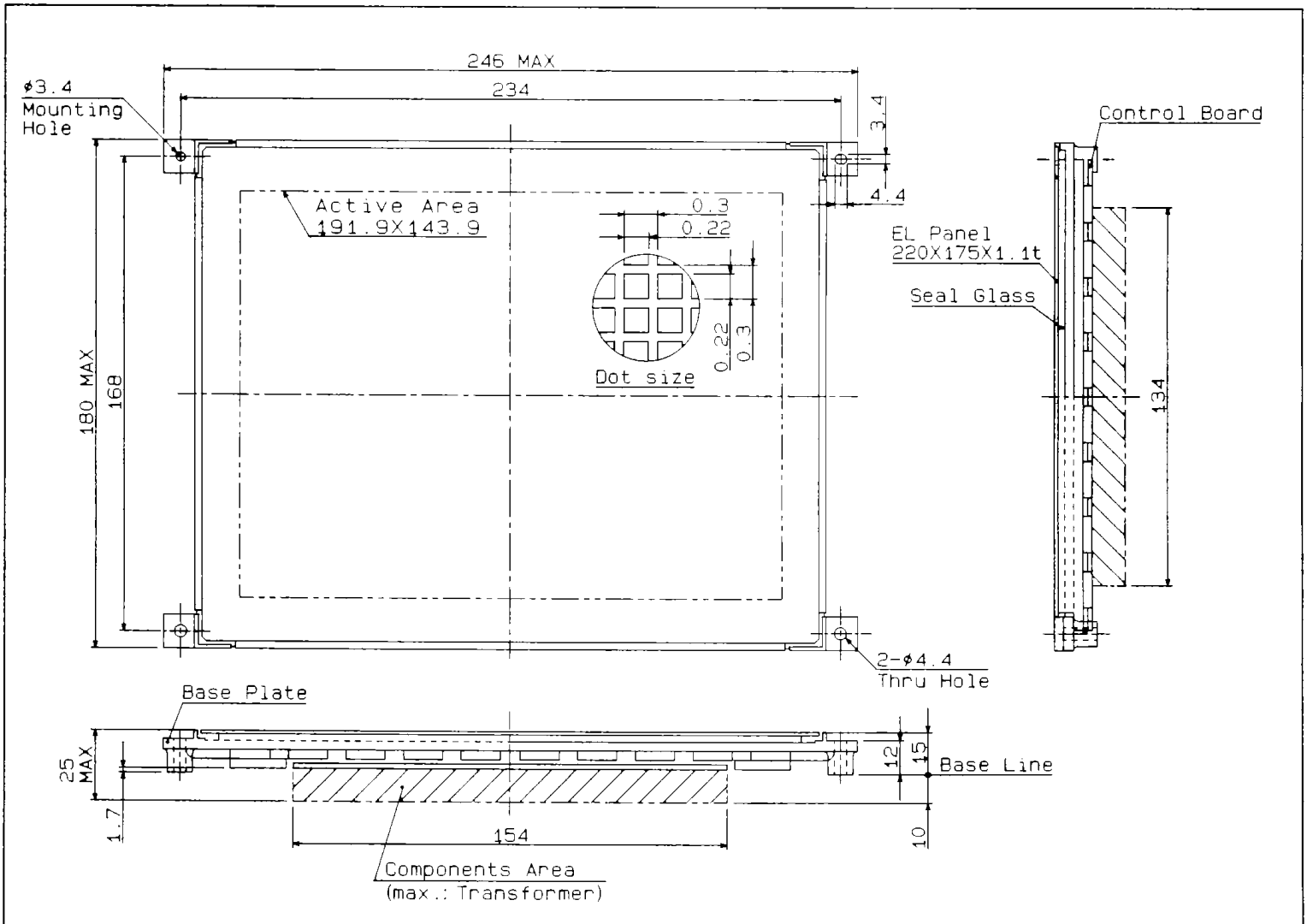
(Ta=25°C)

Parameter	Symbol	Rating	Unit
Interface signal (Logic "H")	V_{IH}	5.5	V
Interface signal (Logic "L")	V_{IL}	−0.5	V
Supply voltage (Logic)	V_L	7	V
Supply voltage (Panel drive)	V_D	27	V
Operating temperature	Topr	0 to +55	°C
Storage temperature	Tstg	−25 to +70	°C

- **Corresponding connector:**
  HIF3BA-16D-2.54R (HIROSE) or equivalents

Outline Dimensions

Unit:mm



Connector
HIF3FB-16PA-2.54DS (HIROSE ELECTRIC) or equivalents.

Electro-optical Characteristics

(Ta=25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	V_L	—	4.75	5.0	5.25	V
Supply current (Logic)	I_L	V_L=5V	100	—	300	mA
Supply voltage (Panel drive)	V_D	—	22.8	24.0	25.2	V
Supply current (Panel drive)	I_D	V_D=24V	40	—	850	mA
Power consumption	P_T	V_L=5V, V_D=24V	—	17	—	W
Luminance	B_{ON}	All dots lit	20	—	—	fL
Off luminance	B_{OFF}	All dots turned off	—	—	1.0	fL
Luminance distribution	$\triangle B_{DIS}$	All dots lit	—	—	35	%

Interface Signals

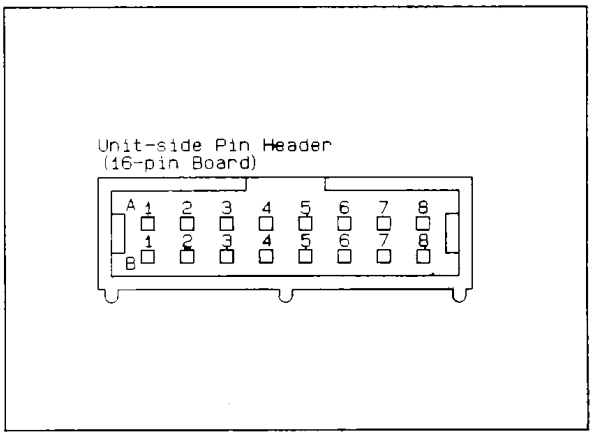
Pin No.	Symbol	Description
A-1	$D_{IN}0$	Data signal for odd column
B-1	$D_{IN}1$	Data signal for even column
A-2	CKD	Data transfer clock
B-2	GND	Ground
A-3	H.D	Horizontal sync. signal
B-3	GND	Ground
A-4	V.D	Vertical sync. signal
B-4	N.C	—
A-5	GND	Ground
B-5	GND	Ground
A-6	V_D	+24V
B-6	V_D	+24V
A-7	V_L	+5V
B-7	V_L	+5V
A-8	N.C	—
B-8	N.C	—

Interface Timing Ratings

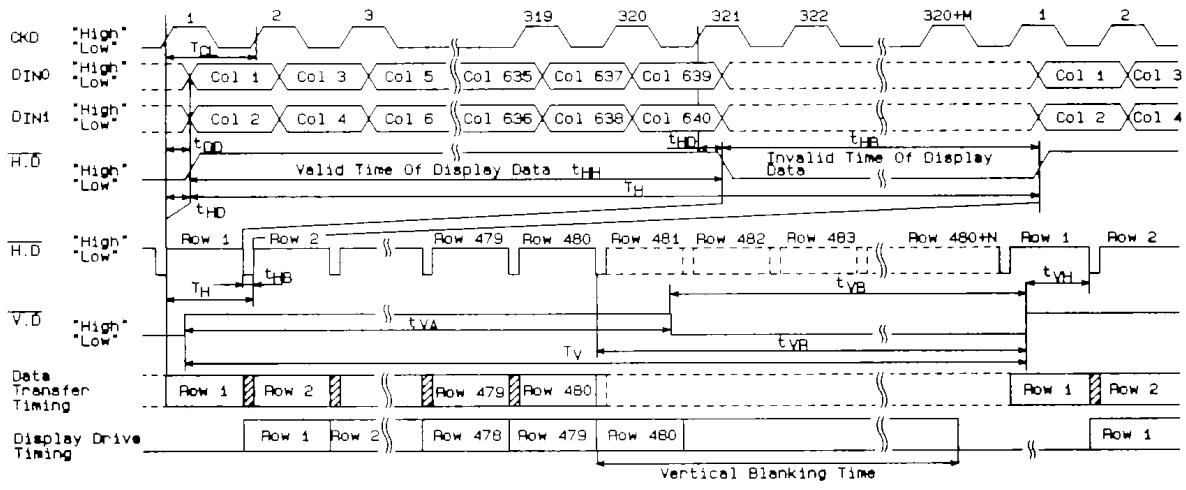
(Ta=25°)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	$1/T_{CL}$	8	—	12.0	MHz
Clock duty	$T_{CL}(H)/T_{CL}\times 100$	45	—	55	%
Horizontal sync. signal cycle time	T_H	34	—	41.3	μsec
Horizontal sync. signal blanking time	t_{HB}	1.3	—	—	μsec
Vertical sync. signal blanking time	t_{VB}	1	—	$N\times T_H$	μsec
Vertical sync. signal valid time	t_{VA}	$480\times T_H$	—	—	μsec
Frame frequency	$1/T_V$	50	—	60	Hz
Data signal delay time required	t_{DD}	0.01	—	T_{CL}	μsec
Horizontal sync. signal delay time required	t_{HD}	0.01	—	$T_{CL}/2$	μsec
Vertical sync. signal rise wait time	t_{VR}	4×34	—	—	μsec
Vertical sync. rise timing	t_{VH}	34	—	$T_H-t_{HB}+29$	μsec

Connector



Interface Timing Chart



LJ64ZU49

Features

- **Display format:** 640 (W) × 480 (H) dots
- **Dot pitch ratio:** 1:1
- 16-Level gray scale
- **Input signal level:** LS TTL level
- **Drive method:** PWM symmetric drive
- **Structure:** Baseplate
- Detachable DC/DC converter
- **Net weight:** Approx. 620g (700g*)
  *Including DC/DC converter

Absolute maximum ratings

(Ta=25°C)

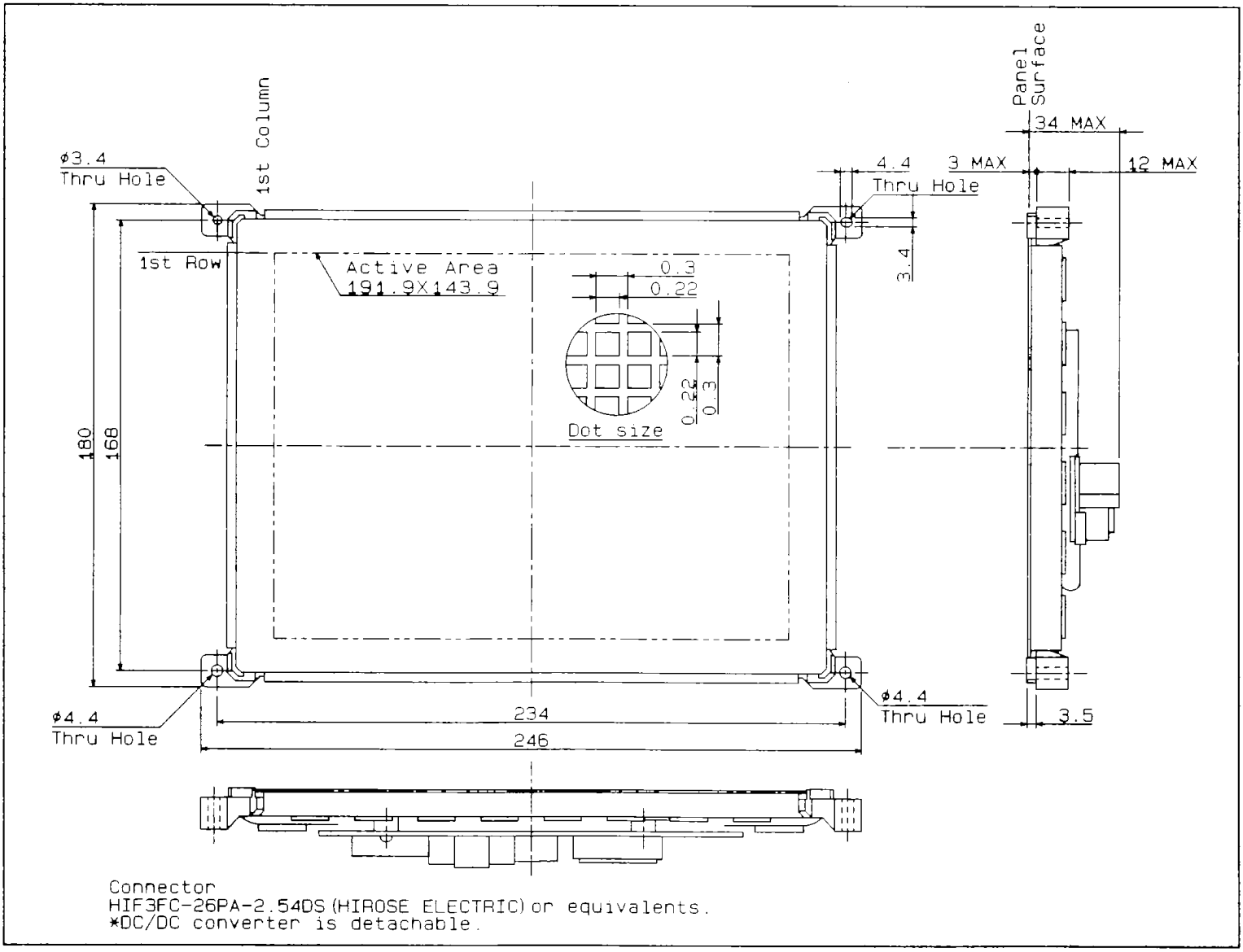
Parameter	Symbol	Rating	Unit
Interface signal (Logic "H")	V_{IH}	5.5	V
Interface signal (Logic "L")	V_{IL}	−0.5	V
Supply voltage (Logic)	V_L	7	V
Supply voltage (Panel drive)	V_D	27	V
Operating temperature	Topr	−5 to +55	°C
Storage temperature	Tstg	−40 to +80	°C

Corresponding connector:

HIF3BA-26D-2.54R (HIROSE) or equivalents

Outline Dimensions

Unit:mm



Electro-optical Characteristics

(Ta=25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	V_L	—	4.75	5.0	5.25	V
Supply current (Logic)	I_L	V_L=5V	100	—	350	mA
Supply voltage (Panel drive)	V_D	—	22.8	24.0	25.2	V
Supply current (Panel drive)	I_D	V_D=24V	400	—	1500	mA
Power consumption	P_I	V_L=5V, V_D=24V	—	22	—	W
Luminance	B_{ON}	All dots lit	23	30	—	fL
Off luminance	B_{OFF}	All dots turned off	—	—	1.0	fL
Luminance distribution	$\triangle B_{DIS}$	All dots lit	—	—	35	%

Interface Signals

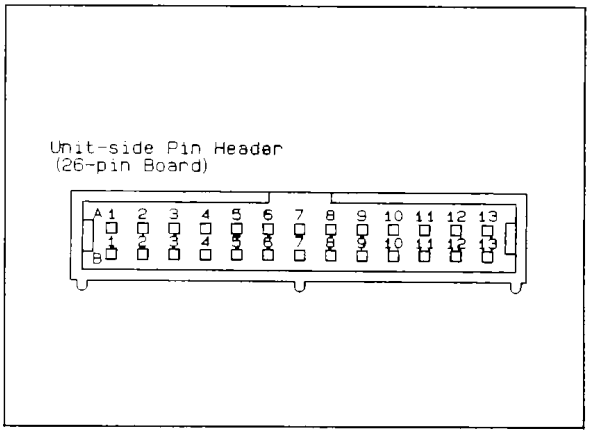
Pin No.	Symbol	Description
A-1	N.C	—
B-1	N.C	—
A-2	D11	Data signal
B-2	D10	
A-3	D13	
B-3	D12	
A-4	D01	
B-4	D00	
A-5	D03	
B-5	D02	
A-6	N.C	—
B-6	N.C	—
A-7	CKD	Data transfer clock
B-7	GND	Ground
A-8	H.D	Horizontal sync. signal
B-8	GND	Ground
A-9	V.D	Vertical sync. signal
B-9	GND	Ground
A-10	GND	Ground
B-10	GND	Ground
A-11	V_D	+24V
B-11	V_D	+24V
A-12	V_L	+5V
B-12	V_L	+5V
A-13	N.C	—
B-13	N.C	—

Interface Timing Ratings

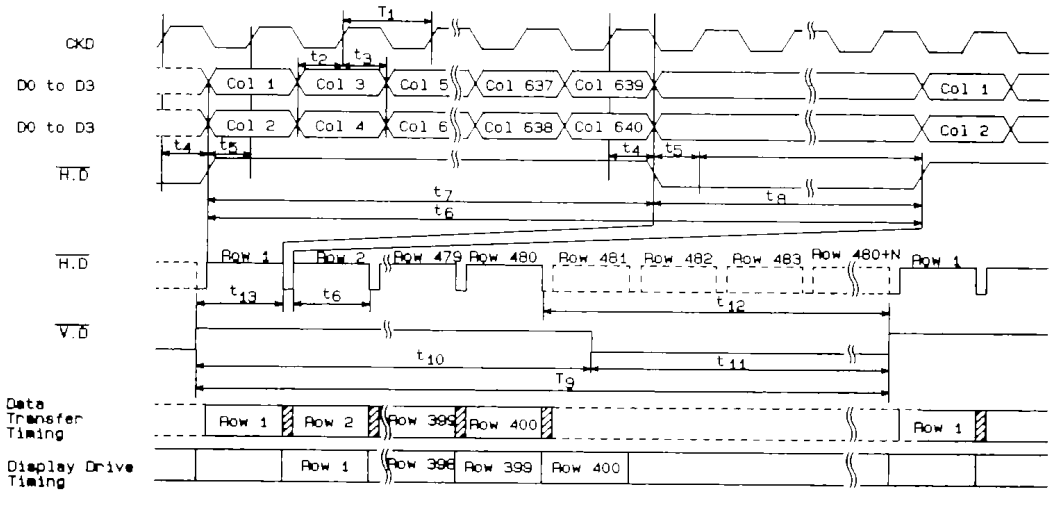
(Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	1/t1	8	—	13	MHz
Clock duty	t1(H)/t1 × 100	45	—	55	%
Data setup time	t2	10	—	—	nsec
Data hold time	t3	10	—	—	nsec
H.D hold time	t4	10	—	—	nsec
H.D setup time	t5	10	—	—	nsec
Horizontal sync. signal cycle time	t6	34	—	41.3	μsec
Horizontal sync. signal valid time (Valid time of display data)	t7		320 × t1		μsec
Horizontal sync. signal blanking time (Invalid time of display data)	t8	1.3	—	—	μsec
Frame frequency	1/t9	50	—	60	Hz
Vertical sync. signal valid time	t10	t6	480 × t6	—	μsec
Vertical sync. signal blanking time	t11	1	—	t9 − t6	μsec
Vertical sync. signal rise wait time	t12	4 × 34	—	—	μsec
Vertical sync. rise timing	t13	34	—	t7+29	μsec

Connector



Interface Timing Chart



LJ720U22

Features

- **Display format:** 720 (W) × 400 (H) dots
- **Dot pitch ratio:** 1:1
- **Input signal level:** LS TTL level
- **Drive method:** P-P symmetric drive
- **Structure:** Baseplate
- **Net weight:** Approx. 850g

Absolute maximum ratings

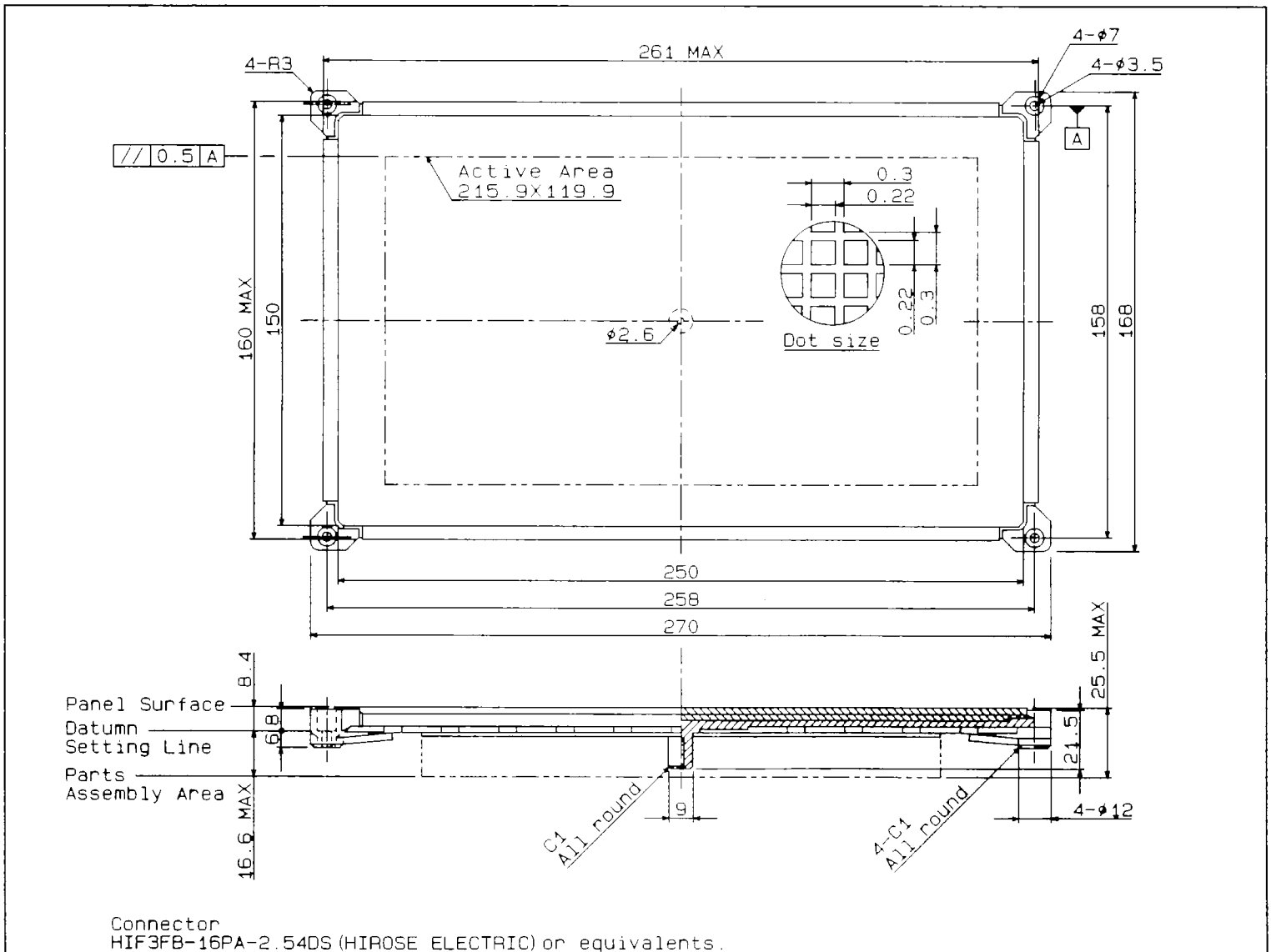
(Ta=25°C)

Parameter	Symbol	Rating	Unit
Interface signal (Logic "H")	V_{IH}	5.5	V
Interface signal (Logic "L")	V_{IL}	−0.5	V
Supply voltage (Logic)	V_L	7	V
Supply voltage (Panel drive)	V_D	18	V
Supply voltage (Panel drive)	V_M	30	V
Operating temperature	Topr	0 to +55	°C
Storage temperature	Tstg	−25 to +70	°C

- **Corresponding connector:**
  HIF3BA-16D-2.54R (HIROSE) or equivalents

Outline Dimensions

(Unit:mm)



Connector
HIF3FB-16PA-2.54DS (HIROSE ELECTRIC) or equivalents.

Electro-optical Characteristics

(Ta=25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	V_L		4.75	5.0	5.25	V
Supply current (Logic)	I_L	V_L=5V	50	—	400	mA
Supply voltage (Panel drive)	V_D		14.25	15.0	15.75	V
Supply current (Panel drive)	I_D	V_D=15V	50	—	600	mA
Supply voltage (Panel drive)	V_M		23.75	25.0	26.25	V
Supply current (Panel drive)	I_M	V_M=25V	25	—	600	mA
Power consumption	P_T	V_L=5V, V_D=15V, V_M=25V	—	13	20	W
Luminance	B_{ON}	All dots lit	20	—	—	fL
Off luminance	B_{OFF}	All dots turned off	—	—	1.0	fL
Luminance distribution	ΔB_{DIS}	All dots lit	—	—	35	%

Interface Signals

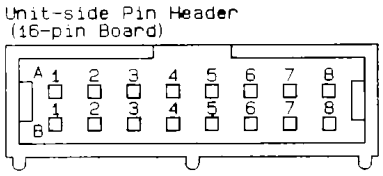
Pin No.	Symbol	Description
A-1	$D_{IN}0$	Data signal for odd column
B-1	$D_{IN}1$	Data signal for even column
A-2	CKD	Data transfer clock
B-2	GND	Ground
A-3	H.D	Horizontal sync. signal
B-3	GND	Ground
A-4	V.D	Vertical sync. signal
B-4	$\overline{\text{RESET}}$	
A-5	GND	Ground
B-5	GND	Ground
A-6	V_M	+25V
B-6	V_M	+25V
A-7	V_L	+5V
B-7	V_L	+5V
A-8	V_D	+15V
B-8	V_D	+15V

Interface Timing Ratings

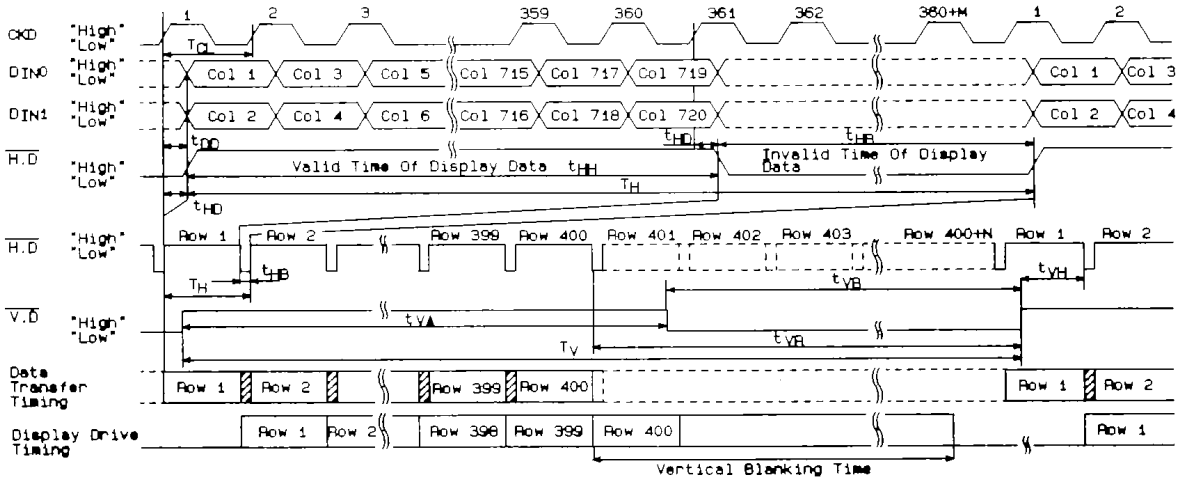
(Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	$1/T_{CL}$	8	10	12	MHz
Clock duty	$T_{CL}(H)/T_{CL}\times 100$	45	—	55	%
Horizontal sync. signal cycle time	T_H	40	—	49	μsec
Horizontal sync. signal blanking time	t_{HB}	1	—	—	μsec
Vertical sync. signal blanking time	t_{VB}	1	—	$N\times T_H$	μsec
Vertical sync. signal valid time	t_{VA}	$400\times T_H$	—	—	μsec
Frame frequency	$1/T_V$	50	60	61	Hz
Data signal delay time required	t_{DD}	0.01	—	T_{CL}	μsec
Horizontal sync. signal delay time required	t_{HD}	0.01	—	$T_{CL}/2$	μsec
Vertical sync. signal rise wait time	t_{VR}	4×40	—	—	μsec
Vertical sync. rise timing	t_{VH}	40	—	$T_{HH}+35$	μsec

Connector



Interface Timing Chart



LJ024U33

Features

- **Display format:** 1024 (W) × 768 (H) dots
- **Dot pitch ratio:** 1:1
- **Input signal level:** H-CMOS level
- **Drive method:** P-P symmetric drive
- **Structure:** Baseplate
- Detachable DC/DC converter
- **Net weight:** Approx. 1050g (1200g*)
  *Including DC/DC converter

■ Absolute maximum ratings

(Ta=25°C)

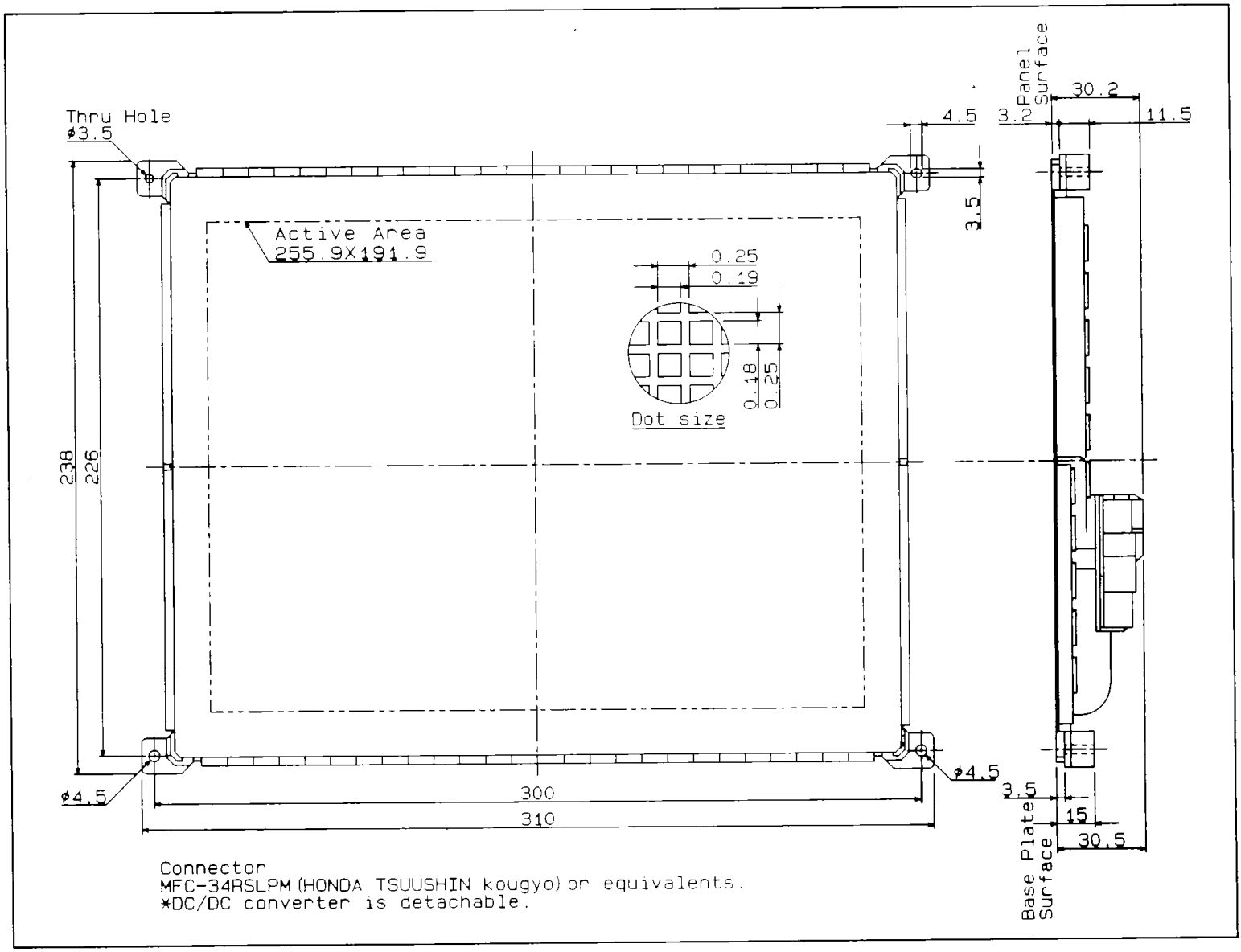
Parameter	Symbol	Rating	Unit
Interface signal (Logic "H")	V_{IH}	V_L +0.5	V
Interface signal (Logic "L")	V_{IL}	−0.5	V
Supply voltage (Logic)	V_L	7	V
Supply voltage (Panel drive)	V_D	27	V
Operating temperature	Topr	0 to +55	°C
Storage temperature	Tstg	−25 to +70	°C

■ Corresponding connector:

MFC-34RPF/MFC-34RPFC or equivalents
(Honda Tsuushin Kougyo)

Outline Dimensions

(Unit:mm)



Electro-optical Characteristics

(Ta=25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	V_L	—	4.75	5.0	5.25	V
Supply current (Logic)	I_L	V_L=5V	200	—	700	mA
Supply voltage (Panel drive)	V_D	—	22.8	24.0	25.2	V
Supply current (Panel drive)	I_D	V_D=24V	300	—	1800	mA
Power consumption	P_T	V_L=5V, V_D=24V	—	31	—	W
Luminance	B_{ON}	All dots lit	23	32	—	fL
Off luminance	B_{OFF}	All dots turned off	—	—	1.0	fL
Lumiance distribution	$\triangle B_{DIS}$	All dots lit	—	—	35	%

Interface Timing Ratings

(Ta=25°C)

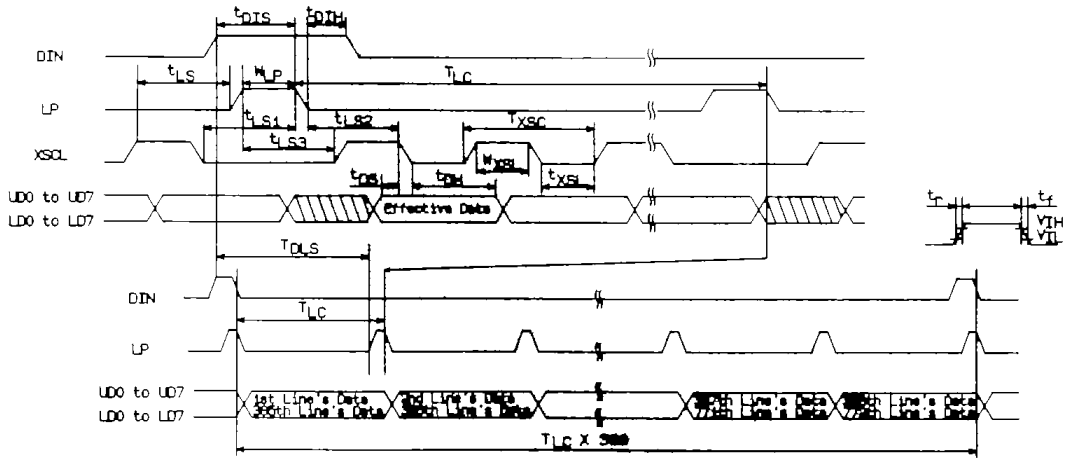
Parameter	Symbol	Min.	Typ.	Max.	Unit
Latch period	T_{LC}	35.6	37.0	38.8	μsec
XSCL period	T_{XSC}	125	—	—	nsec
LP pulse width	W_{LP}	70	—	—	nsec
XSCL "L" time	T_{XSL}	—	60	—	nsec
XSCL pulse width	W_{XSC}	—	60	—	nsec
Latch timing	T_{LS1}	200	—	—	nsec
	T_{LS2}	200	—	—	
	T_{LS3}	100	—	—	
	T_{LS}	10	—	—	
Data setup time	T_{DS}	30	—	—	nsec
Data hold time	T_{DH}	30	—	—	nsec
DIN setup time	T_{DIS}	100	—	—	nsec
DIN hold time	T_{DIH}	20	—	—	nsec
Input signal rise time	t_r	—	—	*	nsec
Input signal fall time	t_f	—	—	*	nsec

* $(T_{XSC}-T_{XSC}-W_{XSC})/2$ 30 nsec max.
* $T_{DLS}>31\mu$sec, $T_{DIS}<31\mu$sec

Interface Signals

Pin No.	Symbol	Description
1	V_L	Power supply for logic (+)
2	V_L	Power supply for logic (+)
3	GND	Ground
4	GND	Ground
5	N.C	—
6	DIN	Sync. pulse
7	LP	Latch pulse
8	GND	Ground
9	XSCL	X shift clock
10	GND	Ground
11	UD0	8th display data signal
12	UD1	7th display data signal
13	UD2	6th display data signal
14	UD3	5th display data signal
15	UD4	4th display data signal
16	UD5	3rd display data signal
17	UD6	2nd display data signal
18	UD7	1st display data signal
19	GND	Ground
20	LD0	8th display data signal
21	LD1	7th display data signal
22	LD2	6th display data signal
23	LD3	5th display data signal
24	LD4	4th display data signal
25	LD5	3rd display data signal
26	LD6	2nd display data signal
27	LD7	1st display data signal
28	GND	Ground
29	GND	Ground
30	GND	Ground
31	GND	Ground
32	V_D	Power supply for panel drive
33	V_D	Power supply for panel drive
34	V_D	Power supply for panel drive

Interface Timing Chart



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